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MODEL 9100-D
LOGIC ANALYZER

OPERATING AND SERVICE MANUAL

MP MASTER

MA34611

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GOULD

OPERATING AND SERVICE MANUAL

MODEL 9100-D

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SECTION I

GENERAL INFORMATION

1.1 Certification

Gould Inc. certifies that this instrument was thoroughly tested and inspected and found to meet its published specifications when it was shipped from the factory.

1.2 Warranty

All Gould Inc. products are warranted against defects in materials and workmanship. This warranty applies for one year from the date of delivery, or, in the case of certain major components listed in the operating manual, for the specified period. We will repair or replace products that prove to be defective during the warranty period. If a unit fails within thirty days of delivery, Gould Inc. will pay all shipping charges relating to the repair of the unit. Units under warranty, but beyond the thirty day period, should be sent to Gould Inc. prepaid and Gould Inc. will return the unit prepaid. Units out of the one year warranty period, the customer will pay all freight charges. IN THE EVENT OF A BREACH OF GOULD INC.'S WARRANTY, GOULD INC. SHALL HAVE THE RIGHT IN ITS DISCRETION EITHER TO REPLACE OR REPAIR THE DEFECTIVE GOODS OR TO REFUND THE PORTION OF THE PURCHASE PRICE APPLICABLE THERETO. THERE SHALL BE NO OTHER REMEDY FOR BREACH OF THE WARRANTY. IN NO EVENT SHALL GOULD INC. BE LIABLE FOR THE COST OF PROCESSING, LOST PROFITS, INJURY TO GOODWILL, OR ANY SPECIAL OR CONSEQUENTIAL DAMAGES. THE FOREGOING WARRANTY IS EXCLUSIVE OF ALL OTHER WARRANTIES, WHETHER EXPRESSED OR IMPLIED, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

1.3 Instrument Description

The Model 9100-D is a high speed logic recorder that has sophisticated triggering and a large memory.

The analyzer compares the nine input signals against user-selected logic thresholds and assigns a binary state of "1" or "0" for each, which is then recorded in a solid-state memory. The comparison and subsequent recording is performed simultaneously on all nine inputs, eliminating input-to-input time skew. Comparison and recording of the input is performed on a sampling basis. The sampling rate is controlled by the period of the internal or external clock.

Recording is under user control and can be changed to capture information prior to, after, or both prior to and after a user defined trigger. The trigger can be defined as a 9-bit pattern to be found in the data. This data trigger can be expanded to 30 bits wide.

The 9100-D's memory length is defined as being 1020 words. A 9100-D word is one simultaneous sampling of all nine data inputs. The 9100-Ds memory length can be converted from samples to time by multiplying by the sampling period of the clock.

Once the memory has been filled, the recorded information can be displayed on a CRT or oscilloscope. The data display is in a timing diagram format. Recorded information may also be withdrawn from the logic analyzer in a binary format for analysis by other digital equipment.

1.4 Specifications

DATA

Inputs. 9.

Impedance. 1 MΩ /10 pF.

Input Mode. Selectable Sample or Latch. Two input mode switches.

Channels 1-4 controlled independently from channels 5-9.

SAMPLE. Unit stores the detected logic level at each active clock edge, simultaneously for all input channels. Minimum pulse width always detected and recorded is one clock plus 2 ns with 250 mV or more threshold voltage overdrive.

LATCH. Detects and flags in memory threshold transitions between active clock edges. The latch's flag is a pulse opposite in state to that stored at the previous active clock edge. The latch will detect transitions of the threshold with pulse widths as narrow as 5 ns and a threshold overdrive of 250 mV.

Setup and Hold Time. Setup = 2 ns. Hold = 1 ns with respect to the clock's active edge. (Externally clocked operation only.)

Skew. Channel-to-channel record time skew less than 2 ns.

Thresholds. Two threshold switches. Channels 1-4 controlled independently from channels 5-9. Selectable thresholds of TTL, ECL and user VARIABLE. Each threshold has two positions, one for X1 probes (black line) and one for X10 probes (red line).

Threshold Voltage:

TTL	+1.4 V
ECL	-1.3 V
VARIABLE	+2.5 to -2.5 V (10-turn pot)

CLOCK

Internal. 100 Hz to 100 MHz. Selectable clock intervals 1,2,5 steps, from 10 ms to 0.01 μs.

Output. A TTL compatible output that is capable of driving one gate. Rate controlled by the front panel controls.

External. Input via front panel BNC connector.

IMPEDANCE. 1 MΩ /10 pF.

THRESHOLD. Selectable via the threshold switch for data input channels 5-9.

RATES. DC to 70 MHz unqualified, DC to 50 MHz qualified.

PULSE WIDTH. Minimum 5 ns.

SLOPE. Active edge selectable positive or negative.

QUALIFIER. One dedicated clock qualifier via a front panel BNC connector.

IMPEDANCE. 1 MΩ /10 pF.

THRESHOLD. Selectable by threshold switch for channels 5-9.

STATES. Selectable "1", "0" or "X" (don't care).

RATE. 50 MHz maximum.

PULSE WIDTH. 10 ns minimum.

SETUP AND HOLD TIMES. 6 ns and 4 ns respectively relative to the active clock edge chosen.

TRIGGER

Sources. Manual, or selection of Internal True, Internal False, or External.

Manual. Priority trigger via front panel switch.

Int (T). The unit is triggered when the input data matches the user-defined Combinational Trigger, the Trigger Qualifier and the rear panel Trigger Inputs (when used).

Int (F). The unit is triggered when the input data ceases to match the user-defined Combinational Trigger, the Trigger Qualifier and the rear panel Trigger Inputs (when used).

Combinational Trigger. A 9-bit data word defining the unit's trigger. Each bit is settable to a logic "1", "0" or "X" (don't care).

COMBINATIONAL TRIGGER EXPANSION. The 9100-D's Combinational Trigger can be expanded to 30 bits by using the trigger qualifier and the addition of two 10-TC accessories. The 9100-D is equipped with accessory DC Power and Trigger Inputs for two 10-TC accessories.

TRIGGER QUALIFIER. One dedicated Trigger Qualifier via front panel BNC connector.

Impedance. 1 MΩ /10 pF.

Threshold. Selectable by threshold switch for channels 5-9.

States. Selectable "1", "0" or "X" (don't care).

Pulse width. One clock period plus 2 ns.

Setup and Hold Time. Setup = 2 ns; hold = 1 ns with respect to the clock's active edge.

External. The unit is triggered only via the two rear panel Trigger Input connectors or rear panel data connector input. The internal Combinational Trigger is disabled.

THRESHOLD. TTL (+1.4 V) positive pulse. Input is internally pulled up. External device must hold input low, except when triggering the unit.

Pulse Width. One sample period minimum plus 2 ns.

Display Marker. Raised step at trigger point on data trace when trigger is recorded (Pretrigger Record mode). Step width varies with display expansion.

Trigger Output. A TTL compatible output, that is capable of driving one gate. The output is normally low and goes to a "1" level upon trigger recognition. The trigger output is a function of the 9100-D's front panel COMBINATIONAL TRIGGER ANDed with the rear panel TRIG INs.

ARM

Selectable Auto, Single and External.

Auto. Unit automatically arms itself after 15 display cycles.

Single. Unit manually armed via front panel switch.

Ext. Unit armed via rear panel BNC connector.

INPUT. TTL level, positive-going pulse. Input is internally pulled up. External device must hold input low, except when arming the unit. Pulse width shall be 1 us minimum.

Arm Output. A TTL compatible output that is capable of driving one gate. The output is normally low, going high for 600 ns in response to either a manual or electrical arm signal.

MEMORY

1024 9-bit words. Memory elements are static RAMs.

RECORD MODES

Selectable Pretrigger, Clock Delay and Event Delay.

Pretrigger. The unit starts recording at arming. The unit stops recording after the pretrigger delay (user selectable) has been saved, the trigger has been recognized, and remaining memory has been filled with new data.

Range. 0-999.

Clock Delay. The unit starts recording after the trigger has been recognized, and the delay count (user selectable) +1 has been counted out.

The unit stops recording after the memory has been filled with new data.

Range. 0-9999.

Event Delay. The unit starts recording at arming. The units stops recording after 200 words of information preceding the Nth trigger (user selectable) +1 have been recorded, and the remaining 824 words of memory have been filled with new data.

Range. 0-9999.

DISPLAY (INTERNAL)

Three function LED display, decimal notation, selectable for the Trigger Delay, Cursor, and △Cursor readings. Specific reading is chosen by depression of the desired function button.

Delay. When selected for the LED readout, delay is in clock intervals for the Pretrigger and Clock Delay record modes. When operating in the Event Delay record mode, delay units are trigger occurrences (or events). Incrementing or decrementing the amount of delay is controlled by the three-speed INC/DEC switch.

Range. Pretrigger = 0-999, Clock and Event Delay = 0-9999.

Cursor. Used for highlighting data in display. When selected for LED readout the cursor position indicated in relative to word one of the memory. Moving cursor to the right or left in memory is controlled by the INC/DEC switch.

Range. 0-999.

Display Marker. Vertical line indicating position.

△Cursor. Used as a reference marker for measurements between it and the Cursor. Reference position is established by setting the △ Cursor via the SET/CLEAR switch. When cleared, the △ Cursor moves with the Cursor. When △Cursor is selected for LED readout, the absolute difference between the Cursors is indicated in clock intervals.

Range. 0-998.

Display Marker. A set △Cursor is evident as a pulse of constant width on each trace, independent of display expansion.

DISPLAY OUTPUTS

X Output. Repetitive 1 V p-p, 1 ms ramp. Period 2 ms.

Y Output. Repetitive nine-segment stair step ramp, each step equally spaced. Data for each channel modulates one step. Full range 0-0.8 V. Each step has a period of 2 ms with data for 1 ms. Data synchronized with the X ramp.

Z Output. A zero to +2.5 V minimum, 1 ms wide pulse. The pulse period is 2.0 ms. The pulse is synchronized such that it is 0 V while the X ramp rises from 0 to 1.0 V. Blanking is timed to occur when the pulse is at +2.5 V.

$\overline{Z}$ Output. A +2.5 V to zero 1 ms wide pulse. The pulse period is 2.0 ms. The pulse is synchronized such that it is 2.5 V while the X ramp rises from 0 to 1 V. Blanking is timed to occur when the pulse is at 0 V.

Format. Nine traces, channel 1 at the top of the display. Horizontal display selectable, X1, MIX or EXPAND.

X1. 1000 bits of recorded data display per trace.

MIX. Used in conjunction with the Cursor. Data to the left of the Cursor is not expanded, while data to the right of the Cursor is expanded under control of the HORIZ EXPAND switch.

EXPAND. Used in conjunction with the Cursor. Only data to the right of the Cursor is displayed and expanded via the Horizontal Expand switch. The Cursor relocates to the left edge of the display.

HORIZONTAL EXPAND. Selectable X5, X10, and X20. Functional only in the Mix and Expand display modes.

DIGITAL INTERFACE

This output allows user access to the recorded data in its binary form.

Format. TTL level signals that are bit-parallel word serial. Each word is 9 bits wide. A total of 1020 words of recorded data can be accessed.

Rates. DC to 200K words/s.

Interface Control. COMMAND. A TTL zero level places the logic analyzer in the digital output mode.

REQUEST. A TTL negative-going pulse requests one data word from the logic analyzer.

FLAG. A TTL positive level from the logic analyzer indicates the data word is valid.

MISCELLANEOUS

Operating Temperature. Range 0-50^{o}C.

Power Input. 100, 117 or 234 VRMS $\pm$ 10%, 50-60 Hz.

Power Consumption. 100 Watts.

10-TC ACCESSORY DC POWER OUTPUTS (2).

Voltage	Current
+5	0.750 A max (TOTAL)
-5	0.250 A max (TOTAL)
GND	

Size.

HEIGHT	5.2"	(13.2 cm)
WIDTH	12.75"	(32.4 cm)
DEPTH	19.0"	(48.3 cm)

Weight. 28 lbs (12.7 kg)

SECTION II

INSTALLATION

2.1 Introduction

This section contains information on unpacking, inspection, repacking, storage, and installation of the Model 9100-D.

2.2 Unpacking and Inspection

Inspect instrument for shipping damage as soon as it is unpacked. Check for broken knobs and connectors; inspect cabinet and panel surfaces for dents and scratches. If the instrument is damaged in any way or fails to operate properly, notify the carrier immediately. For assistance of any kind, including help with instruments under warranty, contact your local Gould Inc., Biomatipn Division, representative or the Gould Inc., Biomation Division, factory.

2.3 Storage and Shipment

To protect valuable electronic equipment during storage or shipment, always use the best packaging methods available. Contract packaging companies in many cities can provide dependable custom packaging on short notice. A factory approved shipping carton can also be obtained by contacting Gould Inc., Biomation Division.

2.4 Power Connection

The 9100-D may be used on a wide range of power line voltages. The rear panel combination fuse holder and power selection switch allows the power selections listed in Table 2.1.

Table 2.1 Line Voltage Selections

Range (+10%)	Fuse (Amp Slow Blow)
100	1
117	1
234	0.5

CAUTION: Before plugging the unit into AC power, verify that the line power select PCB in the fuse holder compartment has been switched to the proper line voltage.

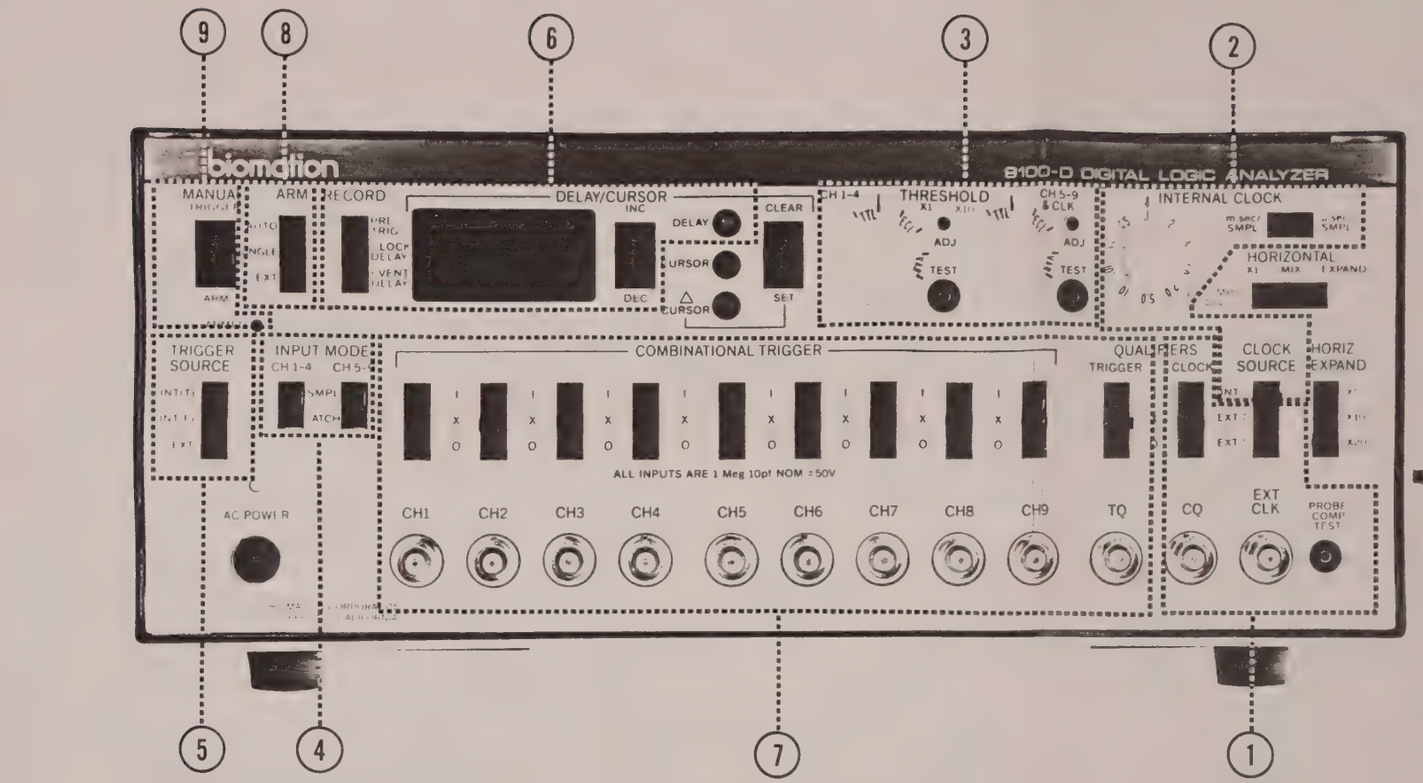
Line voltage selection is achieved by inserting the PCB in the fuse holder compartment, such that the desired line voltage can be read on the top of the PCB when inserting.

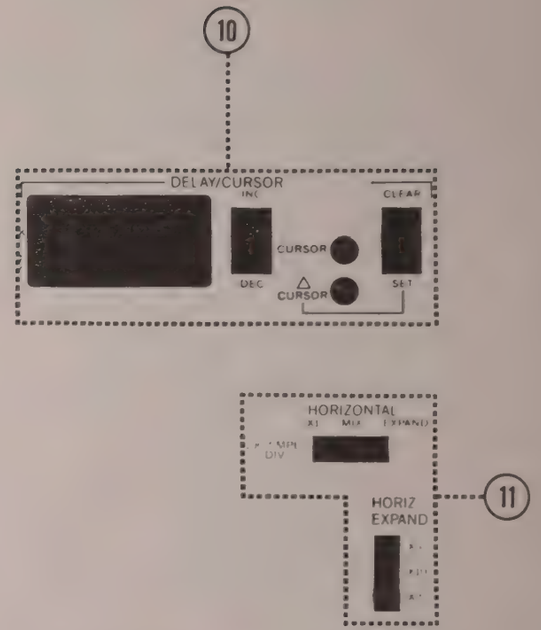
2.5 Preparation for Use

The Model 9100-D can be operated in a self-contained system by simply connecting it to a CRT display or oscilloscope. The following sections of this manual cover operation and setups.

2.6 Initial Warm-up

Although the Model 9100-D is a solid-state instrument, a brief warmup period of approximately 10 minutes is required for the internal circuitry to reach thermal stabilization.





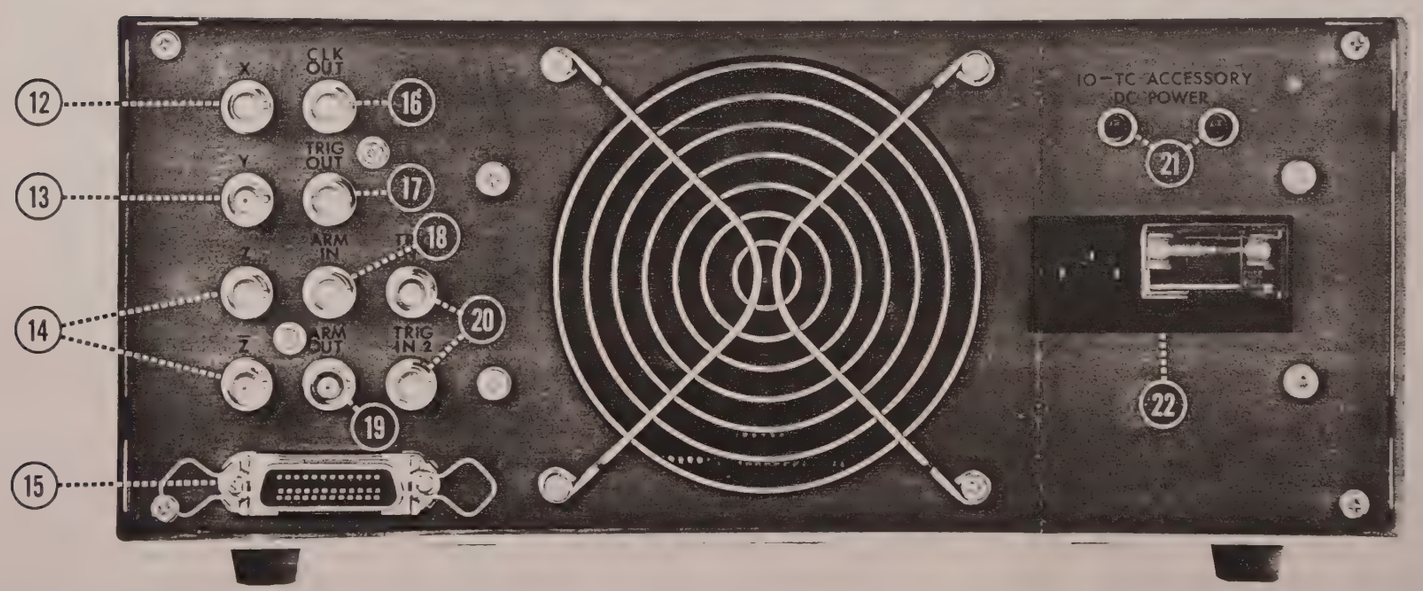
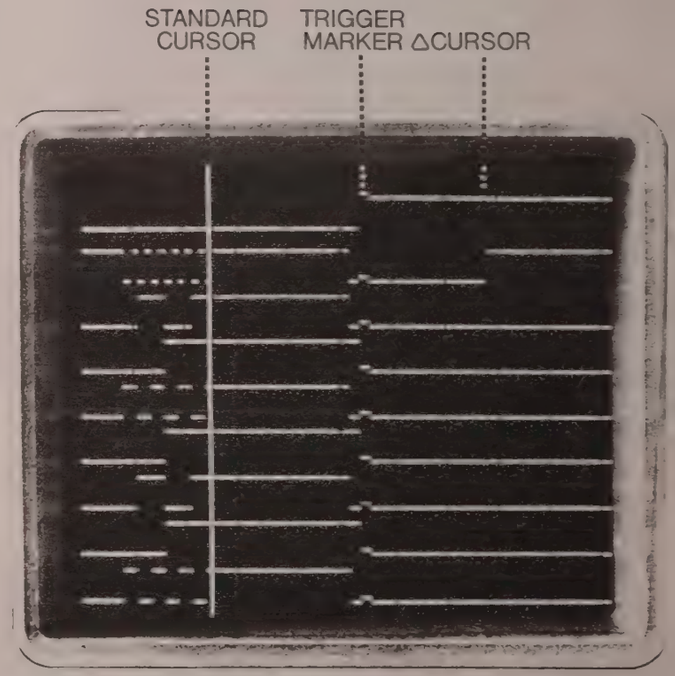


Figure 3.1 Front and Rear Panels of the 9100-D



TYPICAL DISPLAY

SECTION III

OPERATION

3.1 Introduction

This section explains the use and function of the front panel controls and inputs as well as the rear panel inputs and outputs. It also offers the user a step-by-step procedure for operating the unit.

3.2 Front Panel Controls and Inputs

Refer to Figure 3.1 while reviewing this section.

(1) EXTERNAL CLOCK INPUT, CLOCK SOURCE, CLOCK QUALIFIER AND PROBE COMPENSATION TEST POINT

The External Clock input allows the user to input an external clock into the logic analyzer to make synchronous logic recordings. To clock the 9100-D from an external clock the Clock Source switch must be in one of the two external positions. The two external clock positions allow the user to select the clock edge on which data is recorded.

The External Clock may be qualified with a system signal by using the Clock Qualifier (CQ) input. The switch above CQ allows the user to select on which state the qualifier gates the external clock. The state choices are "1", "0" and "X" (don't care). When an external clock is used and no qualifying is required, the state selector for the CQ input should be in the "X" position.

NOTE: When a clock signal synchronized with the system under test is used for external clocking of the 9100-D, a fixed record clock/data signal phase relation exists. In this case, data signals with information rates up to one-half the clock rate can be recorded.

The External Clock input is also used in conjunction with the Probe Compensation Test Point for adjusting X10 compensatable probes used with the 9100-D.

The following is a procedure for compensating the probes.

a. Connect the uncompensated logic analyzer probe to the External Clock input. The probe tip should be connected to a suitable square wave generator or scope calibrator.

b. A scope should be connected to the Probe Compensation Test Point with a properly compensated scope probe.

c. View the square wave on the scope and adjust the logic probe compensation capacitor to obtain a crisp (minimizing overshoot and undershoot) square wave.

d. Repeat this procedure for all probes to be used with the logic analyzer.

(2) INTERNAL CLOCK

The 9100-D has its own crystal controlled clock that allows the user to make asynchronous recordings. The Clock Source selection switch must be in the Internal position to make the 9100-D's Internal Clock selection switches functional. These switches control the period and units at which the input data is sampled, compared, and recorded. By manipulation of the Internal Clock switches, maximum and minimum input sampling periods of 10 ms and 0.01 μs respectively can be obtained.

An important factor to remember in working with this logic analyzer is that it is a sampling device. The analyzer samples its data inputs at the active clock edge. The result of the sampling is stored in memory.

NOTE: When internal clocking is used, no fixed phase relationship exists between the system clock/data signals and the 9100-D's internal clock. To minimize the effects of this changing phase relationship, the clock interval for the 9100-D should be one-tenth the interval of the minimum pulse to be recorded. As the clock interval for the 9100-D approaches that of the data to be recorded, errors in recorded pulse widths will occur.

(3) THRESHOLD

The 9100-D has two threshold switches for selecting preset and variable thresholds. Each signal input is compared against the threshold setting selected at these switches. Input signals that are more positive than the threshold selected are assigned a binary "1" state. Input signals that are more negative than the selected threshold are assigned a binary "0" state. These threshold switches have provisions at each threshold for X1 and X10 probes. The black lines are the positions for X1 probes. The red lines are the positions for X10 probes. The preset thresholds and their values are: TTL = +1.4 V, ECL = -1.3 V.

The variable position allows the user to adjust the threshold that suits his system best. Adjusting the threshold is achieved via the 10-turn potentiometer labeled ADJ on the front panel. The probe tip threshold the user has adjusted is monitored at the test point labeled TEST. The monitor ground should be connected to the shell of input BNC #5.

The 9100-D has two threshold switches to allow the user the flexibility of recording two IC technologies simultaneously. The first threshold switch controls thresholding for channels 1-4. The second threshold switch controls thresholding for Channels 5-9, the Trigger and Clock Qualifiers, and the External Clock.

(4) INPUT MODE

The 9100-D has two input mode switches. These switches allow the user to turn on or off the unit's glitch (narrow noise spike) capturing capability to suit the logic system under test. Channels 1-4 are controlled independently from Channels 5-9. Each switch has two positions, Sample and Latch.

In the Sample position, the unit will ignore threshold transitions between active clock edges. The Sample mode will find greatest usage when recording in synchronous logic systems. Synchronous logic makes decisions at active system clock edges and is immune to logic changes that occur between these clock edges.

Asynchronous logic is not clocked and responds to virtually any threshold transition even if it is noise. Knowing that narrow noise spikes exist in an asynchronous logic system is of great value.

The Latch mode detects and flags in the analyzer's memory any threshold transitions that occur between the clock edges. The 9100-D can detect noise spikes as narrow as 5 ns with a 250 mV overdrive. (Note that the shortest period between clock edges for the analyzer is 10 ns.) Noise spikes between clock edges are flagged in memory as a one clock interval wide pulse, opposite in state to the previously clocked state. Figure 3.2 demonstrates both the Sample and Latch input modes.

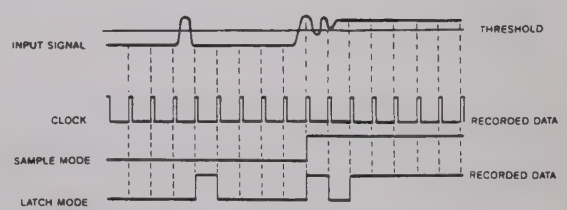


Figure 3.2 Sample and Latch Input modes.

The Latch mode indicates the presence of noise spikes and their time occurrence relative to the other recorded information. The period of the noise spike is not indicated by the latch mode flag.

(5) TRIGGER SOURCE

This three-position switch allows the user to define which trigger inputs are used for triggering the 9100-D.

When in the Int (T) position the 9100-D is triggered when the unit's front panel Combinational Trigger, and rear panel Trig In 1 and 2 become true. All these triggers are logically ANDed..

Circuitry internal to the 9100-D recognizes if any of the rear panel trigger inputs are unused and substitutes a trigger signal to those inputs. In the Int (T) position, the Trig In 1 and 2 can be used to expand the unit's front panel Combinational Trigger input. With two 10-TC accessories, the 9100-D's Combinational Trigger can be expanded by 20 bits.

In the INT (F) mode the 9100-D is triggered when the Combinational Trigger, rear panel Trig In 1, or Trig In 2 singularly or collectively become false. The 9100-D recognizes any unused rear panel trigger inputs and substitutes a trigger signal to those inputs. The two rear panel Trig In inputs can be used to expand the unit's Combinational Trigger by 20 bits.

The 9100-D is triggered from Trig In 1 and 2 when operated in the Ext Trigger Source position. Again unused inputs are recognized and supplied automatically with a trigger signal.

NOTE: The Digital Output connector trigger input is wired to TRIG IN 1; therefore, the Digital Output connector trigger input may be used in place of TRIG IN 1. TRIG IN 1 and the Digital Output connector trigger input may not be used at the same time.

(6) RECORD MODES, DELAY/CURSOR LED DISPLAY, INC/DEC SWITCH, AND THE DELAY FUNCTION BUTTON

This logic analyzer has three recording modes; Pretrigger, Clock Delay, and Event Delay.

PRETRIGGER

Pretrigger recording allows the user to record information prior to the user-defined trigger event (5). By use of the Delay/Cursor LED display, the Delay function button and the INC/DEC switch, the user can define the allocation of pretrigger and post-trigger information in any recording. To make a Pretrigger recording where 200 words of pretrigger memory are saved, the following switch settings are required.

a. The 9100-D is placed in the Pretrigger Record mode.

b. The Delay function button is depressed. The button lights. (The LED display's function is controlled by the three-function buttons adjacent to the display. The Cursor and △Cursor function buttons are discussed in paragraph 10.) Now the Delay/Cursor display will indicate the clock intervals or words of pretrigger data to be saved.

c. Increment or decrement the three-speed INC/DEC switch to obtain the 200 words of pretrigger information to complete this set-up. Note that in the Pretrigger Record mode the maximum amount of pretrigger information that can be saved is 999 words.

d. The 9100-D memory has a 1020 word long memory. The first 1000 words are viewable on a scope or CRT; 1020 words of data are available at the Digital Output connector. With 200 words of memory allocated to pretrigger information, 800 words of post-trigger information can be viewed on a CRT.

Pretrigger recording is extremely helpful in troubleshooting. For example, the user defines an erroneous address on the unit's Combinational Trigger and makes a Pre-trigger Recording saving 200 words of pre-trigger and 800 words of post-trigger information for viewing.

The pretrigger information tells the user how he arrived at the erroneous address while post-trigger information identifies where the system proceeded after the error.

CLOCK DELAY

Clock Delay recording is designed for recording information that occurs after the trigger. The beginning of the analyzer's recording can be delayed with respect to the trigger by use of the Delay/Cursor LED display, the Delay function button, and the INC/DEC switch. The amount of delay on the LED display introduces delay between the trigger and start of recording in units of the selected clock interval. A Clock Delay recording that is delayed 35 clock intervals after the trigger would require the following switch settings.

a. The 9100-D is placed in the Clock Delay Record mode.

b. The Delay function button is depressed and lights. Now the Delay/Cursor display will indicate the clock intervals of delay between the trigger and the beginning of the recording.

c. Increment or decrement the INC/DEC switch to obtain 34, one less than the desired delay of 35. The 9100-D has 1 clock interval of static delay in the Clock Delay mode, which added to 34 achieves the desired result of 35 intervals of delay. Note that the maximum amount of Clock Delay that can be selected is 9999 clock intervals.

EVENT DELAY

Event delay recording is designed for recording information that occurs after numerous occurrences of an event or trigger. The beginning of the analyzer's recording can be delayed by occurrences of the trigger with the use of the Delay/Cursor LED display, the Delay function button, and the INC/DEC switch. The amount of delay on the LED display introduces delay between the trigger and the start of recording in occurrences of the trigger. An Event Delay recording in which the analyzer would begin recording after 5 trigger occurrences would require the following control settings.

a. The 9100-D is placed in the Event Delay Record mode.

b. The Delay function button is depressed. Now the Delay/Cursor display will indicate the number of trigger occurrences required before the unit begins recording.

c. Increment or decrement the INC/DEC switch to obtain 4, one less than the desired trigger occurrence delay of 5. The 9100-D has 1 trigger occurrence of static delay in the Event Delay record mode. Therefore, the LED reading of 4 plus the 1 trigger occurrence of static Delay gives the desired 5 trigger occurrences of Event Delay.

   Note that the maximum Event Delays that can be selected on the LED display are 9999.

d. The data of an Event Delay recording is allocated relative to the Nth (user selected) +1 trigger occurrence as follows; 200 clock intervals of pretrigger information and 800 clock intervals of post-trigger information will be displayed.

NOTE: The 9100-D will operate in the Event Delay Record mode only when the Trigger Source switch is in an INT position (INT(T) or INT(F)).

Event Delay recording is especially useful for making recordings after a specific number of similar occurrences, for example a peripheral address.

(7) COMBINATIONAL TRIGGER AND TRIGGER QUALIFIER AND TRIGGER MARKER.

The 9 parallel bit Combinational Trigger enables the analyzer to be triggered from input data. The user defines each bit of the data trigger as either a "1", "0" or "X" (don't care). The input for each data bit is directly below its trigger state switch. The 9100-D has a Trigger Qualifier (TQ). The Trigger Qualifier is ANDed with the 9-bit combinational trigger. The user can define the state of the Trigger Qualifier as "1", "0" or "X". The input for the Trigger Qualifier is directly below the state switch. When the trigger qualifier is not used, its state switch should be placed in the "X" position.

Expansion of the unit's combinational trigger is achieved by use of the Trigger Qualifier and/or the two rear panel TRIG INs. Remember that the unit's Trigger Source switch must be positioned in Int (T) or Int (F) to expand the combinational trigger.

The 9100-D has a display trigger marker that appears on a CRT or scope screen as a small pulse superimposed on each data channel at the trigger point. See Figure 3.1. Of course, the trigger event must have been recorded by the 9100-D to mark it; therefore, the trigger marker is only viewable when operating the 9100-D in the Pretrigger Record mode. The Trigger Marker is affected by horizontal expansion, which helps to distinguish it from the △ Cursor.

(8) ARM

Arming the logic analyzer is the first step performed in preparing the unit for recording. When the logic analyzer is in the Pretrigger or Event Delay Record mode, arming the unit begins the recording process; the analyzer finds the proper trigger, assures that the proper allocation of pretrigger and post-trigger information has been saved, stops recording, and goes into the display mode. When the logic recorder is in the Clock Delay mode, arming the unit simply alerts the unit to look for the trigger. Once the trigger has been found and the delay has been counted out, recording begins. Recording ends when the memory has been filled with new data. Then the logic analyzer goes into the display mode.

When the 9100-D is in the Auto Arm mode, the unit displays the memory contents 15 times and then automatically rearms itself. This mode of arming is useful for setting up the instrument and tracking changing circuit conditions.

The Single arm position requires the user to rearm the unit manually before each recording. This Arm mode is the most commonly used. This mode will preserve data in the logic analyzer's memory until the user purposely initiates another recording by rearming the unit.

The External Arm position allows the 9100-D user to electrically arm the unit. An arm signal is input to the unit via the rear panel (ARM IN connector).

Because arming the 9100-D is a necessary step before recording, arming may be used as a condition for triggering the analyzer. A 10-TC accessory will give the user combinational triggering capability for arming the 9100-D. The arming 10-TC's trigger output connector would be connected to the 9100-D's rear panel ARM IN. The 9100-D could be triggered from the data. Now, the 9100 will be armed when the 10-TC trigger becomes true and triggered when the 9100-D's combinational trigger becomes true.

(9) MANUAL TRIGGER/ARM AND ARM INDICATOR LED

This momentary switch allows the user to manually Arm or Trigger the 9100-D. Both the Arm and Trigger are priority inputs recognized immediately by the 9100-D.

The Manual Trigger will be helpful for setting up logic analyzer test. By arming and triggering the unit after probes have been connected to the system under test, the user may check for proper signal continuity to the analyzer prior to beginning the tests.

The ARM LED will light when the 9100-D has been manually or electrically ARMED. The LED is extinguished when a trigger has been detected and recording is complete.

(10) CURSOR,△CURSOR,INC/DEC SWITCH, and DELAY/CURSOR LED DISPLAY

The 9100-D features two cursors and a LED display that enables (1) exact positioning of the cursor in the memory and (2) exact time measurements.

CURSOR

By use of the Delay/Cursor LED display, the cursor function button and the INC/DEC switch, the user can move the cursor (vertical bar) to any point in memory and read its exact location on the LED display. To move the cursor to the 58th stored word in the 9100-D's memory, the following operations are necessary.

(a) Push the Cursor button. The button will light indicating that the LED display is reading the cursor's position.

(b) Increment or decrement the INC/DEC switch to obtain the desired cursor position read out on the Delay/Cursor LED display (58). While incrementing or decrementing the INC/DEC switch, note the vertical bar cursor moving on the CRT or scope screen. Remember that the cursor position can only be changed by the INC/DEC switch when the cursor button is lit.

The 9100-D's cursor plays a key role in the HORIZONTAL MIX and EXPAND modes of operation. See paragraph 11. The cursor also plays a large role in the operation of the △CURSOR.

△CURSOR

The △Cursor is a reference cursor that allows exact measurements between itself (△Cursor) and the 9100-D's standard cursor. The △Cursor appears on the display as a narrow pulse superimposed upon each of the 9 recorded data signals. See Figure 3.1. When using any of the horizontal expansions, the △Cursor remains at a constant pulse width. Placement of the △Cursor is accomplished by use of the INC/DEC switch, the CURSOR button, △CURSOR button and the CLEAR/SET switch. The following steps are required to set the △Cursor and make a time measurement.

(a) Actuate the Clear/Set switch, clear direction, clearing the △Cursor. Once cleared the △Cursor moves with the standard cursor. Remember to push the Cursor button so the standard cursor can be moved. Move the standard Cursor to the desired area of the display for time measurement (for example one end of a recorded data pulse).

(b) Actuate the Clear/Set switch, set direction, setting the △Cursor.

The △Cursor will become visible after the standard cursor is moved.

(c) Up until this time the Delay/Cursor LED display has been giving the user a readout on the position of the standard cursor in the 9100-D's memory. Depressing the △Cursor button zeros the LED display.

(e) Any incrementing of decrementing of the INC/DEC switch will move the standard cursor. The LED display will give the user a constant update of the absolute number of clock intervals (internal or external) between the standard and △ cursor. The relative difference between the cursors will be available on the LED display as long as the △Cursor button is activated (lit). Depressing the Delay or Cursor buttons will change the LED display to that function's read out; however, depressing the △Cursor button will give the user the difference, in clock intervals, between the cursors once again.

(f) The clock intervals displayed on the Delay/Cursor LEDs can be converted to time by multiplying by the period of the clock.

Use of the HORIZONTAL MIX mode of operation and X5, X10 or X20 HORIZONTAL EXPAND in conjunction with Cursor/△Cursor measurements makes positioning of the cursors easier, especially if the measurements are made with the standard cursor to the left of the △Cursor. See Figure 3.1.

(11) HORIZONTAL modes and HORIZONTAL EXPAND

These two, three-position switches allow convenient horizontal expansion of the timing diagram display.

HORIZONTAL EXPAND

This switch controls the horizontal expansion factor of the display when the 9100-D is in either the HORIZONTAL MIX and EXPAND modes. Expansions of X5, X10, and X20 are available.

HORIZONTAL modes

This switch controls the horizontal display mode of the recorded data.

X1

In the X1 position, 1000 clock intervals of data are displayed horizontally across the CRT or scope screen. For a 10 cm graticule 100 clock intervals of recorded data would be displayed per division. The user views the entire memory in this mode.

MIX

When operating in the MIX HORIZONTAL mode the user will observe that data on the display to the left of the standard bar cursor has a X1 expansion. Data to the right of the standard cursor is expanded by a factor of X5, X10 or X20 controlled by the HORIZONTAL EXPAND switch. The cursor controls where the expansion factors change. The cursor can be moved in the MIX mode allowing expanded analysis of the recorded data. The X1 area to the left of the cursor or the Delay Cursor LED display serves as a constant reminder of where the cursor is in the 9100-D's memory.

EXPAND

In the Expand mode of operation, only the data to the right of the cursor in the X1 or MIX modes of operation is displayed on the screen. The number of clock intervals, of data viewable in the EXPAND mode, are a function of the HORIZONTAL EXPAND switch setting. Fifty, 100 or 200 clock interval of data can be viewed by selecting X20, X10 or X5 HORIZONTAL EXPANDs respectively. Of course, the entire 1000 clock interval memory can be viewed by incrementing or decrementing the cursor.

3.3 Rear Panel Inputs and Outputs

(12) X OUTPUT

This output is used in obtaining a CRT or scope display of the 9100-D recorded information. This output serves as horizontal drive for the CRT and scope display. See Section 1.4 for the X Output specifications. See Section 3.4 for interfacing to this output.

(13) Y OUTPUT

This output is used when displaying the 9100-D's recorded information on a CRT or scope. This output contains the recorded data and serves as the vertical drive for the CRT and scope display. See Section 1.4 for the Y Output specifications. See Section 3.4 for interfacing to this output.

(14) Z and $\overline{Z}$ Outputs

These outputs are used when displaying the 9100-D's recorded information on a CRT or scope. They provide the retrace blanking drive for CRT and scope operation. See Section 1.4 for the Z and $\overline{Z}$ Output specifications. See Section 3.4 for interfacing to these outputs.

(15) DIGITAL OUTPUT

This connector enables the user to access the 9100-D memory and the recorded data contained there. The recorded digital information is available in its binary form. The data output through this connector is bit-parallel word serial. Data Output 1 corres-

the data recorded on channel 1 and data output 9 corresponds to data recorded on channel 9. See Section V for a complete specification of the data output signals as well as the other control input/output signals available at this connector.

(16) CLOCK OUT

The frequence of the clock signal at this point is controlled by the front panel INTERNAL CLOCK. The maximum useable output frequency at this point is 50 MHz.

(17) TRIG OUT

This output is low until the front panel COMBINATIONAL TRIGGER and the rear panel TRIG IN 1 and 2 are recognized. The TRIG OUT operates in this manner regardless of the TRIGGER SOURCE selectors position (INT (T), INT (F) or EXT).

(18) ARM IN

This input allows arming of the unit electrically. This input is wired to an ARM IN pin on the DIGITAL OUTPUT connector (15). Only one arm input may be used at a time.

(19) ARM OUT

This output is normally low, going high for 600 ns in response to either a manual or electrical (ARM IN) arm signal.

(20) TRIG IN 1 and 2

These two inputs each serve a dual function. (1) each allows triggering of the 9100-D from a single, TTL level signal, TRIGGER SOURCE EXT. The 9100-D is triggered on a TTL "1" level. Recall that TRIG IN 1 is wired to a trigger input signal on the DIGITAL OUTPUT connect (15). Only one TRIG in may be used at a time. (2) Also individually or combined the TRIG INs allows expansion of the 9100-D's combinational trigger. Wtih two 10-TC Probe Pod Accessories, the 9100-D's combinational Trigger can be expanded to 30 bits, TRIGGER SOURCE INT.

(21) 10-TC ACCESSORY DC POWER

These connectors supply the DC power necessary for operating 10-TC Probe Pod Accessories.

(22) POWER INPUT CONNECTOR AND FUSE HOLDER

The 9100-D may be used on a wide range of power line voltage, see Table 2.1 for the selections and proper fuse.

Line voltage selection is achieved by inserting the PCB in the fuse holder compartment, such that the desired line voltage can be read on the top of the PCB.

3.4 Set-up Procedure and Operation

3.4.1 This section diagrams the connection of a 9100-D to oscilloscopes and CRTs. See Figures 3.3 a, b and c.

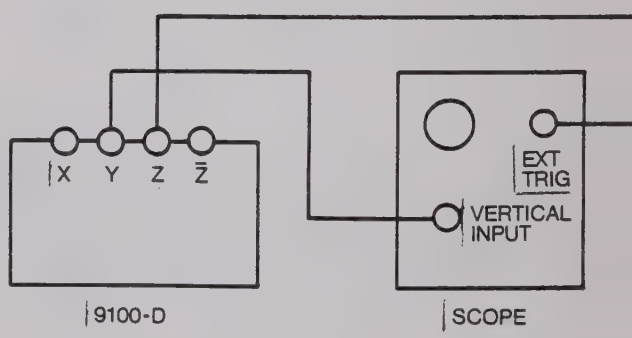


Figure 3.3a Interconnection Diagram

Oscilloscope Settings Y-Z Operation	
Vertical sensitivity:	0.1 V/div, DC coupled.
Vertical position:	Nine traces evenly spaced on the screen.

Horizontal sweep:	100 μs/div.
Horizontal position:	Allowing viewing of 1000 clock intervals of data.
External trigger sensitivity:	1.0 V, DC coupled.
External trigger slope:	Negative slope.

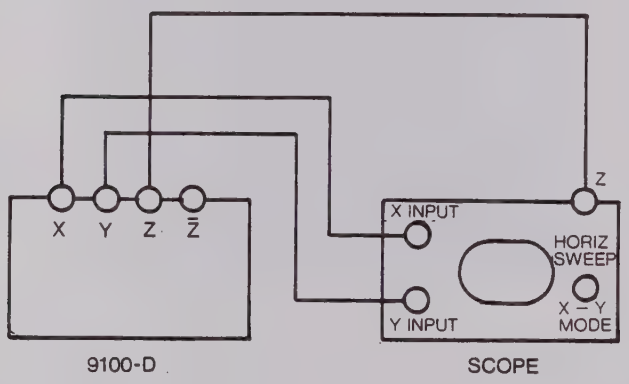


Figure 3.3b Interconnection Diagram

Oscilloscope Settings
X-Y Operation

Y Sensitivity:	Approximately 0.1 V/div, DC coupled.
Y Position:	Nine traces evenly spaced on the screen.
Vertical mode:	X-Y
X Sensitivity:	0.1 V/div, DC coupled.
X Position:	Adjusted to allow viewing of 1000 clock intervals of data.

Horizontal sweep:	X-Y Mode
Retrace blanking:	Choose Z or $\bar{Z}$ to ensure the display beam is blanked after the X ramp returns to zero volts.

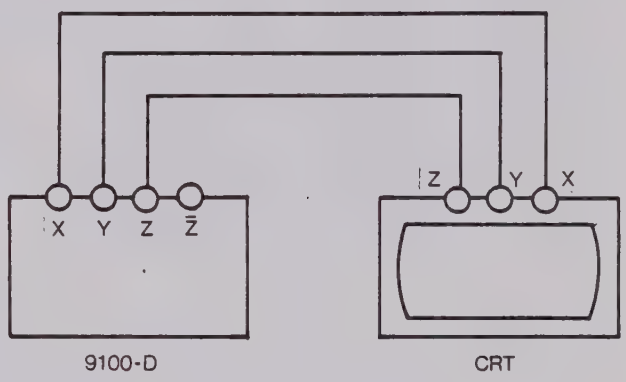


Figure 3.3c Interconnection Diagram

CRT Settings
X-Y-Z Operation

Vertical sensitivity:	Approximately 0.1 V/div, DC coupled.
Vertical position:	Nine traces evenly spaced on the screen.
Horizontal sensitivity:	0.1 V/div, DC coupled.
Horizontal position	Adjusted to allow viewing of 1000 clock intervals of data.

Retrace blanking: Choose Z or $\overline{Z}$ to ensure the display beam is blanked after the X ramp returns to zero volts.

3.4.2 This section is supplied to give the user a better understanding for the operation of the 9100-D. This section is divided into three discussion that correspond and add to the discussion of section 3.2 paragraph (6) with the same title.

The data recorded by the 9100-D in the following discussions are produced with a pulse generator that has a manual, single pulse output mode. The high and low levels of the pulse are TTL compatible and the pulse width is 1.0 μs. The generator is connected to channel 1 of the 9100-D.

Duplicating these discussions and variations of them enhances user familiarity and understanding of the 9100-D.

PRETRIGGER

To make a pretrigger recording saving 200 clock intervals of information prior to the trigger the set up must be performed exactly as indicated in the PRETRIGGER paragraphs of Section 3.2 (6). The following table lists the 9100-D switch settings not discussed thus far.

Switch	Position
ARM:	SINGLE (Only one recording is desired.)
THRESHOLD: CH 1-4 CH 5-9 and clock	TTL red line (Circuitry under test is TTL and the logic probes are X10).
CLOCK SOURCE:	INT (The circuitry under test is not clocked and high resolution timing information is desired about the circuit outputs.)
INTERNAL CLOCK:	0.01 μs/sample (This clock rate allows 100 samples per the minimum data pulse.)
TRIGGER SOURCE:	INT (T) (The 9100-D will look for the combinational trigger to become valid.)
COMBINATIONAL TRIGGER:	CH 1 = "1" CH 2 - 9 = "X"
QUALIFIER TRIGGER:	"X" (Not used in this recording.)
INPUT MODE: CH 1-4 and CH 5-9	LATCH (This input mode will flag any noise spikes that transition the logic threshold and could cause a circuit malfunction.)
MANUAL TRIGGER/ARM:	ARM (Recording begins with arming when operating in the pretrigger record mode. The display blanks when the 9100-D is armed. When the combinational trigger is found the 9100-D will save 200 words of pretrigger information then continue on recording and save 800 words of post-trigger information. Pulse the generator once. A new display then appears on the screen. See Figure 3.4 for the recorded data and notes concerning the recording).
CURSOR button:	Lit (This enables the user to manipulate the cursor and read its position on the DELAY/CURSOR LED display.)
INC/DEC:	Incremented or Decremented as needed to place the cursor in memory position 195. This placement of the cursor is done to expand the display, allowing maximum visual resol-

ution of the data in the area of the Trigger.

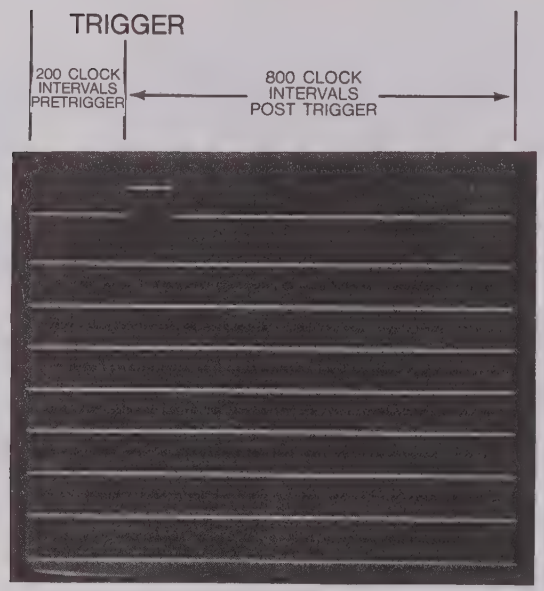


Figure 3.4 PRETRIGGER Recording with 200 Clock Intervals of Pretrigger Information Saved.

HORIZONTAL modes: MIX

HORIZONTAL EXPAND:	X20 (The display has a horizontal magnification of X1 to the left of the cursor and X20 to the right. Timing resolution is easy and accurate in this mode. See Figure 3.5. Note the Trigger marker superimposed on the data.)

This ends the example of the 9100-D/Pretrigger operation.

CLOCK DELAY

This discussion elaborates on the example begun in Section 3.2 paragraph (6) titled CLOCK DELAY. To record data that is exclusively after the trigger, the CLOCK DELAY record mode is used. To make such a recording, where 35 clock intervals of delay between the trigger and the beginning of the recording are required, perform the set up of paragraph (6). The ability to delay a recording from the trigger allows the user flexible placement of the recording. The following table and comments cover switch settings not discussed in paragraph (6).

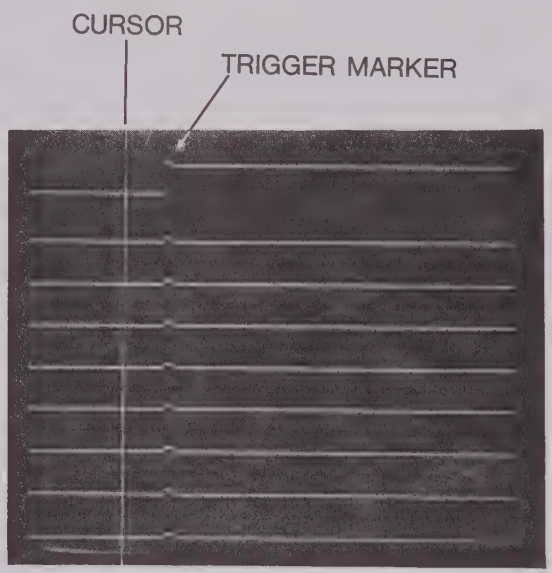


Figure 3.5 PRETRIGGER Recording Showing Data, the Cursor and the Trigger Marker.

SWITCH	POSITION
ARM:	SINGLE (Only one recording is desired.)
THRESHOLDS: CH 1-4 CH 5-9 and CLOCK	TTL, red line (Circuitry under test is TTL and the logic probes are X10.)
CLOCK SOURCE:	INT (The circuitry under test is not clocked and high resolution timing information is desired about the circuit outputs.)
INTERNAL CLOCK:	0.01 μs/sample (This clock rate allows 100 samples per the minimum data pulse.)
TRIGGER SOURCE	INT (T) (The 9100-D will look for the combinational trigger to become valid.)

COMBINATIONAL TRIGGER:	CH 1 = "1" CH 2-9 = "X"
QUALIFIER TRIGGER:	"X" (Not needed; a 1 bit combinational trigger is satisfactory.)
INPUT MODE: CH 1-4 and CH 5-9	LATCH (This mode will flag noise spikes that occur between clock samples.)
MANUAL TRIGGER/ARM:	ARM (Arming the 9100-D in the CLOCK DELAY record mode alerts the unit to look for the combinational trigger. When the trigger is recognized the 9100-D counts the number of clock delays set on the Delay/Cursor LED display (34) plus a one clock interval of static delay. After the delay has been counted out, recording begins. Pulse the generator once. Figure 3.6 shows the resultant recording. Note also the explanatory notes on the figure.

The important points to remember are: (1) The CLOCK DELAY record mode is designed to record information that occurs after the trigger; (2) The amount of delay set into the DELAY/CURSOR delays the beginning of recording from Trigger recognition.

EVENT DELAY

This discussion is offered to elaborate on the example in Section 3.2 paragraph (6) titled EVENT DELAY. Event Delay recording allows delaying the beginning of recording by a user selectable number of trigger occurences. To set up for an Event delay recording of 5 see Section 3.2. The following table and comments cover switch settings not discussed in paragraph (6).

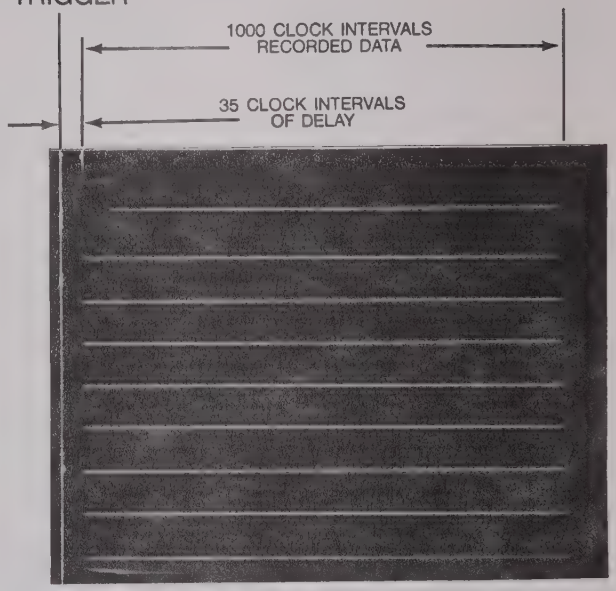


Figure 3.6 CLOCK DELAY Recording With a Delay of 35.

SWITCH	POSITION
ARM:	SINGLE (Only one recording is desired.)
THRESHOLDS: CH 1-4 CH 5-9 and CLOCK	TTL, red line (Circuitry under test is TTL and the logic probes are X10.)
CLOCK SOURCE:	INT (The circuitry under test is not clocked and high resolution timing information is desired about the circuit outputs.)
INTERNAL CLOCK:	0.01 µs/SAMPLE (This clock rate allows 100 samples per the minimum data pulse.)
TRIGGER SOURCE:	INT (T) (The 9100-D will look for the combinational trigger to become valid.)
COMBINATIONAL TRIGGER:	CH 1 = "1" CH 2-9 = "X"

QUALIFIER TRIGGER:	"X" (Not needed; a 1 bit combinational trigger is satisfactory.)
INPUT MODE: CH 1-4 and CH 5-9	LATCH (This mode will flag noise spikes that occur between clock samples.)
MANUAL TRIGGER/ARM:	ARM (Arming the 9100-D in the Event Delay record mode begins the recording process. The unit looks for and counts trigger occurrences. Pulse the generator five times. The 9100-D stops recording 800 clock intervals after the 5th trigger occurrence. The 9100 will save 200 clock intervals of data preceding the 5th trigger occurrence. See Figure 3.7 and the explanatory notes about the recording.

An important feature of Event Delay recording is that the 9100-D gives the user pretrigger and post-trigger information about the Nth+1 (N = user selectable) trigger occurrence.

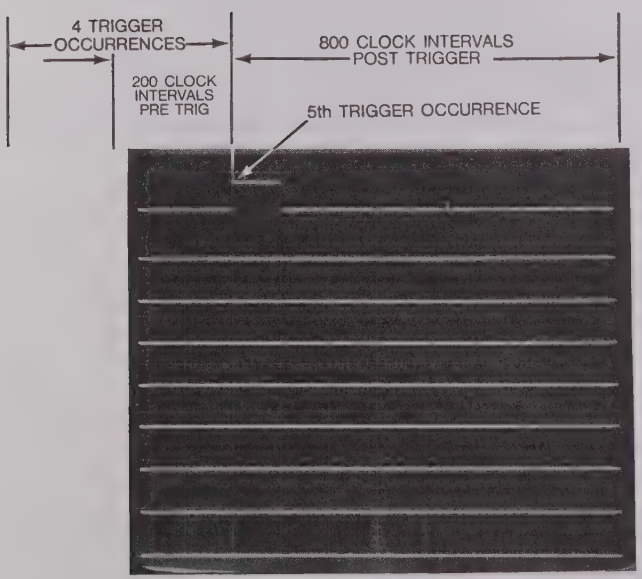


Figure 3.7 EVENT DELAY Recording With a Delay of 5.

SECTION IV

PRINCIPLES OF OPERATION

4.1 Introduction

This section is divided into two parts. The first part gives a block diagram description of the instrument and the second part gives a detailed treatment of the theory of circuit operations.

4.2 Basic General Description

The 9100-D is composed of four subsystems:

1. Power Supply
2. Front Panel Assembly
3. Control Board
4. Main Board

The power supply operates at 100, 117, 200 or 230 VAC, 50 or 60 Hz. It provides +5 V at 7.5 A maximum and -5.2 V at 10 A maximum. A fan is used for cooling.

The front panel has all the operating controls, delay and cursor readouts, and threshold generating circuitry.

The control board has the display control logic and low-speed timing generation logic.

The main board has the high-speed clock and timing generation, record control logic, data inputs, and memory.

Figure 4.1 is a detailed functional block diagram. The front panel control lines are shown at the left, as well as signal inputs. Outputs are shown to the right. I/O commands are also shown to the right. Dotted lines indicate divisions between boards. The LED board is part of the front panel assembly.

The main board receives the data through the buffer/comparators and stores it in the prememory. The record control logic, along with the arm and trigger logic, combinational trigger, and delay counter control the movement of the data from the prememory to the main memory.

The control board generates the display and display controlling signals. When the instrument is recording, the display control logic is held reset. When the recording is done, the display control logic will read data out of the memory and display it. Other signals generated are the cursor and the trigger marker.

The LED board generates the number used in the delay counter and displays it. The four digit LED display is on the front panel. The LED board also generates the △ cursor blip and sends it to the Y DAC on the control board to be displayed. Other functions of the LED display are the cursor position and △ cursor count. Front panel switches and a three-way multiplexer determine which function the LED display is in.

The 9100-D uses three logic families: ECL 10K, Schottky TTL, and CMOS. ECL 10K is used in all high-speed circuitry to achieve 100 MHz performance. Schottky TTL is used in the memory section, since it has adequate performance and is more economical than ECL. CMOS is used in the low-speed display control sections. Low cost and simple interface to ECL make CMOS ideal for this application. The memory subsystem operates off +5 V. All other logic operates off -5.2 V. Positive logic convention is used; i.e., the more positive signals are "1", the more negative are "0". Level translators are necessary to go from ECL or CMOS to TTL, from ECL to CMOS, and from TTL to ECL or CMOS. CMOS will drive ECL directly. Figure 4.2 shows the level translators used.

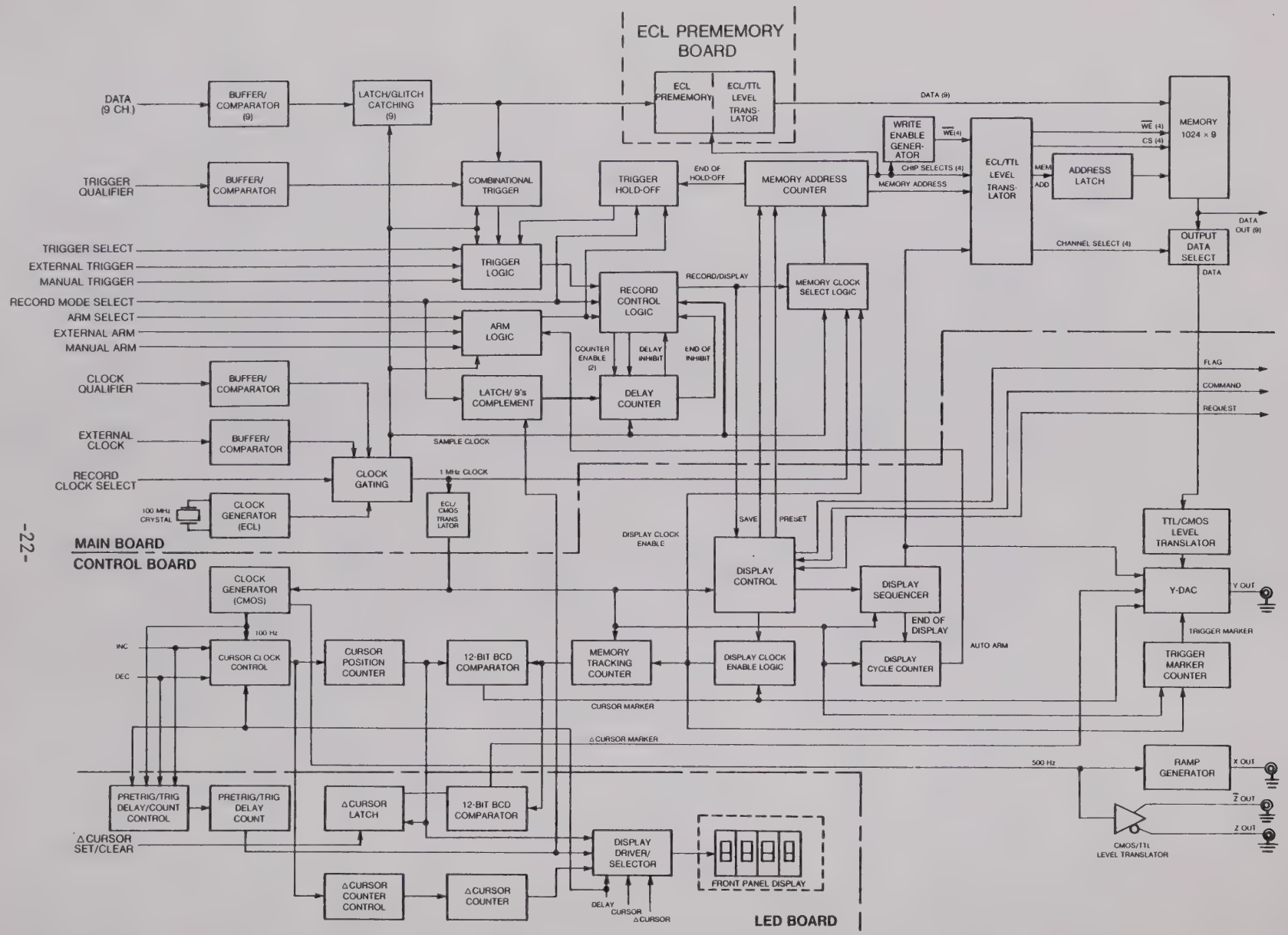


Figure 4.1 Detailed Functional Block Diagram

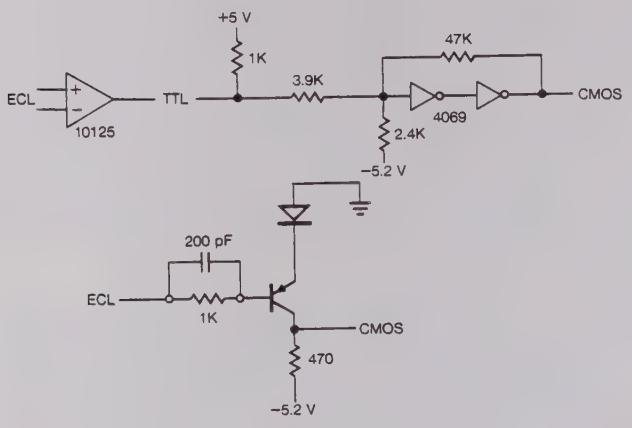


Figure 4.2 Level Translators

4.3 Detailed Description

4.3.1 Front Panel Assembly

The front panel assembly consists of two PC boards and the front panel. The boards are called the "Front Panel Board" and the "LED Board". The front panel board provides the mounting and electrical connections of all operating switches and the LED display. The front panel board connects to the main board and control board by 16-pin ribbon cables and to the LED board by flat cables soldered in. The flat cables may serve as a hinge to provide access to the front panel board. If the 9100-D is operated in this position, a ground connection MUST be made to the LED board from any other board.

4.3.1.1 Front Panel Board

Aside from mounting and connecting all operating switches, the Front Panel Board also contains the threshold voltage circuit. The schematic is shown in Section VIII.

R2 and R7 drop the voltages supplied to R57, R58, R65 and R66 to approximately + 2.8 V. ECL and TTL thresholds are set directly from these voltages by R57 and R58. Variable thresholds are set by R66 (CH 1-4) and R65 (CH 5-9, CQ, TQ, EXT CLK). U2 is a voltage follower used to buffer the pots and eliminate any loading effects. X1 and X10 thresholds are selected by SW1 and SW2, which also select ECL, TTL or VARIABLE. X10 thresholds are generated by switching R67 and R68 in (X10) and out (X1) of the circuit.

U1 is a debouncing circuit for the arm and trigger switch.

4.3.1.2 LED Board

The LED board generates and displays the numbers used for PRETRIG/TRIG delay, the CURSOR number (which is the difference between the CURSOR and the REFERENCE "blip"), and the REFERENCE "blip." 9A, 9C and 9E are used with the LED function select switches. 9E and 9A are connected as SR flip flops. 9C is the gating mechanism for releasing or resetting a previously selected function when another one is selected.

10B, 10C, 11B, 11C, 12B and 12C are data multiplexers that select one of three sources of data for the LED drivers. They are used on the three lower digits. The MSD is not multiplexed since CURSOR and △CURSOR are three digit numbers. Only TRIG DELAY is a four digit number, and only in CLOCK DELAY or EVENTS DELAY modes. In all other modes the MSD is blanked. 10A, 11A, 12A and 13A are BCD-seven segment decoder/driver chips.

10D, 11D, 12D, and 13D are the DELAY COUNT counter circuit. The number generated in this string of counters is used in the DELAY COUNTER, which supports the RECORD CONTROL LOGIC, and is displayed in the DELAY function of the LED display. 13B and 13C serve to stop the counter at 0000 and 9999 to prevent roll-over.

When the counter is counting up to 9999, the 8 bit from 13D generates a high on the one and four parallel input lines of the counters. A CARRY or a BORROW (TC_D) from 13D generates a PARALLEL LOAD pulse for the counters. If the counters are

at 9999, the next clock will load the high on the Q_0("1") and Q_3("4") lines (pins 15 and 9) into the counters. The outputs are forced to hold the 9999 count as long as clocks are fed into the CU input of the chain.

When the counter is counting down, a BORROW (TC_D) is generated at 0000 and appears on pin 13 of 13D. Since the 8 bit is a 0, pins 15 and 9 on all counters are low, and a 0 is loaded into each counter in the chain. This cycle will repeat itself everytime a count down clock is given the counters when the count is 0000.

BC gates the clocks on or off and is used to select which clock is to be used. 5A is a dual D flip flop. The INC and DEC switches are fed into the D inputs. Since the flip flops are clocked at 10 Hz, they effectively debounce the switches. The Q outputs are fed into 8C, selecting either count up or count down clocks. The $\overline{Q}$ outputs are ORed and drive the CET and PE inputs on 5C.

5C is the hesitation circuit. With neither INC nor DEC switch active, both $\overline{Q}$ outputs are high. 4C is a negative input OR gate in which any low will generate a high on the output. 4C-11 is held low. When CET is low, 5C (a 40161) will not count. Also, while CET is low PE is also held low, so the counter loads a 15 (1111_{16}). When either INC or DEC becomes active 4C-11 goes high, pulling CET and PE on 5C high. The counter (5C) can now count. 5C-15 (TC) is high, since a count of 15 is still in the counter. This holds 7C-11 high and enables both halves of 8A.

Q1 and Q3 on 5C are high, so 7A-10 is low. This holds CEP (5C-7) high also enabling the counter. At the next positive transition on the clock line, TC (5C-15) will go low and Q1 and Q3 will go low. 7A-10 stays low, so 7C-11 will go low, disabling both CU and CD clocks. CEP (5C-7) is still high. The counter will continue to count on every positive transition of the clock line. Two clocks later, Q1 goes high. This pulls 7A-10 high. This in turn pulls CEP low, stopping the counter. 7C-11 also goes high, enabling the clocks again. The two counts during which the CU and CD clocks are disabled is the hesitation. It lasts 0.2 s. A timing diagram showing the sequence of events is shown in Figure 4.3.

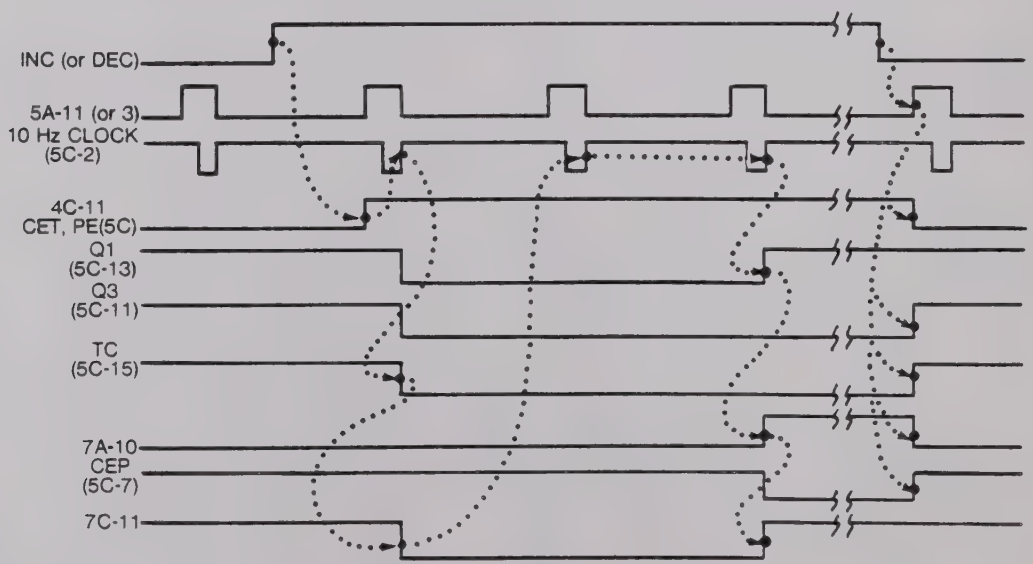


Figure 4.3 Hesitation Circuit Timing Diagram

The DELAY COUNT chain runs at three speeds: 10 Hz for the first 11 to 20 counts (depending on the starting number in the LDS), 50 Hz for the next 60 counts and 200 Hz thereafter. This is accomplished by having a 10 circuit (8A) that divides 100 Hz down to 10 Hz. This counter is then switched over to dividing by 2 and, finally, a 200 Hz clock is selected and the 50 Hz clock returned to 10 Hz operation.

This switching is achieved using 6A, 8A and supporting gates, and 6A is clocked off the 1 bit in the second (tens) digit of the DELAY COUNT chain. At counts 0 and 1 (on 6A), 9C-4 remains low, disabling 4C. 8A operates in the ÷10 mode. From count two to count seven, either or both of the 2 and 4 bits (Q1 and Q2) on 6A is high, and 9C-4 goes high enabling 4C. This allows 8A to parallel load an eight into its parallel inputs each time TC goes high (at a count of nine). 8A will then count between eight and nine, dividing the input 100 Hz clock down to 50 Hz.

At the count of eight on 6A, Q3 will go high, forcing CEP on 6A low. This tops 6A at that count. 6A will be reset to 0 when the INC (or DEC) switch is released and 4C-11 goes low. When Q3 goes high 7A-1 goes high, enabling that gate and passing the 200 Hz clock. At the same time 7A-6 goes low disabling that gate, which was used to pass the 10 Hz and 50 Hz signals.

The △ CURSOR counter counts the absolute number of clock pulses between a settable REFERENCE (or DELTA) CURSOR and the main CURSOR. It consists of 10E, 11E and 12E. 10F, 11F and 12F are used to detect when the △CURSOR count is at 000. 5E, 6E and 7E are a gating structure that determine which direction the main CURSOR is moving and on which side of the REFERENCE CURSOR it is, and therefore whether the △CURSOR counter will count up or down.

The △ CURSOR counter will count up when:

(1) The main CURSOR is to the right of the REFERENCE and the main CURSOR is moving to the right (CURSOR POSITION COUNTER counting up).

(2) The main CURSOR is to the left of the REFERENCE and the main CURSOR is moving to the left (CURSOR POSITION COUNTER counting down).

The △CURSOR counter will count down when:

(1) The main CURSOR is to the right of the REFERENCE and the main CURSOR is moving to the left (CURSOR POSITION COUNTER counting down).

(2) The main CURSOR is to the left of the REFERENCE and the main CURSOR is moving to the right (CURSOR POSITION COUNTER counting up).

5E is a flip flop that is enabled when the △CURSOR counter is at 000. A count-up clock at this time indicates that the main CURSOR is moving to the right and will be to the right of the REFERENCE. This sets 5E-11 low, enabling count up pulses to go to the CU clock input of 10E, and count down pulses to go to the CD clock input of 10E. Condition one of both preceding paragraphs is met.

If a count down pulse is received at 000, then 5E-10 goes low and enables count up pulses to go to the CD clock input and count down pulses to go to the CU clock input. Condition two is met.

7C is used to gate off the CU line when the CURSOR POSITION counter is at 000 or 999, indicating that the CURSOR has reached one end of the display and will remain at that point. 3C senses 999; 3D, 4C and 12F sense 000.

NOTE: From the above description it is clear that the REFERENCE cursor CANNOT be set at either extreme (000 or 999) of the display. If it is set at either extreme, the △ CURSOR measurement will be ONE COUNT LESS than expected.

The LED board also generates the REFERENCE cursor "blip." 2C, 2D and 2E are latches that hold the number from the CURSOR POSITION counter. With pin 5 high, data will pass straight through the latches. 4D is used as an S-R flip flop to control pin 5 on 2C, 2D and 2E. A CLEAR command from the front panel switch or a turn-on clear signal (R10, C22, 13B) will set 4D-15 high. Comparators 1C, 1D and 1E sense an equality between the number at the output of the latches and the memory tracking counter and generate a high. The high at 1C-3 is sensed by 9A-6 and latched in 4D. This edge is fed to the control board to be used in the Y DAC.

A SET command from the front panel switch forces 4D-15 low, latching whatever data is at the input of the latches at the output. This becomes a fixed number that determines the position of the REFERENCE cursor on the display. The equality is sensed and displayed as above.

Note that the reference cursor is always present, but can only be distinguished from the main CURSOR when the two are at different locations.

4.3.2 Control Board

The control board generates the X, Y and Z signal outputs from DATA from the memory, a low-speed (CMOS) timing chain, and a CURSOR POSITION circuit.

The low-speed clock generator consists of 17C, 18C, 19C and 20C. A 1 MHz signal from the Main Board is divided by 10 in each of four stages to produce 100 kHz, 10 kHz, 1 kHz and 100 Hz clocks.

21A is used to debounce the INC and DEC switches. 19B, 19A and 20B form a hesitation circuit identical to the circuit used on the LED board. The circuit provides 320 ms of hesitation.

17B, 20A, 19A and 18B form a clock generator that determines the speed of the cursor clocks (CU and CD) depending on the expansion factor selected. 17B is a $\div 16$ counter and also provides a clock for the hesitation circuit.

The CURSOR POSITION COUNTER consists of 8A, 9A and 10A. CU and CD clocks, selected as described above, drive the circuit. Stops in the form of PARALLEL LOAD (for 999) and RESET (for 000) signals are provided. Power-on reset is also applied to the CURSOR POSITION COUNTER to ensure that the CURSOR comes up at the left edge.

13B, 14B and 11A are the MEMORY POSITION (TRACKING) COUNTER. It counts whenever the DISPLAY CLOCK ENABLE signal is active. 2B, 4A and 3A form a stop that disables the counter at the count of 1020. The same signal generates a "PSEUDO BLANK" signal, which is ANDed into the Y DAC to "blank" the screen when the last bit of information is displayed. This feature is only seen in EXPAND mode.

8B, 10B and 11B are 4-bit comparators cascaded to form a three digit comparator. CR1, CR2 and CR3 are a diode-resistor AND gate that detects an equality in all three comparators. The rising edge of this equality condition is differentiated in R18 and C5 and fed into the Y DAC as a short pulse. This is the main CURSOR. The same equality condition is latched as $M > N$ on the next display clock ($\overline{1\ MHz}$. DISPLAY CLK, EN.). The M>N condition is used to shift from the X1 clock to an expanded clock in MIX mode and to stop the counter at the CURSOR POSITION during the BLANK time in EXPAND mode.

16C is the display control flip flop. It is held reset while the 9100-D is in RECORD. When the RECORD line goes low, indicating that the recording cycle is over, 16C clocks a high through at a time related to the blanking signal. 2 ms later, the second half of 16C clocks this level through. The SAVE signal that latches the last address in the Memory Address Counter into the Save Register is taken off the Q output of the first flip flop. The DISPLAY MODE signal is taken off the second flip flop.

16B and 22B are used to generate the PRESET signals required to initialize the

various counters before displaying each line of data. PRESET (16B-2) generates a DISPLAY CLOCK ENABLE that allows MEMORY ADDRESS COUNTER (on the Main Board) and MEMORY TRACKING COUNTER to advance. PRESET 4 ensures the proper loading of the saved address into MEMORY ADDRESS COUNTER. PRESET 3 allows the TRIGGER POSITION COUNTER to advance.

6B, 5B and 7B form a frequency divider that divides the 1 MHz clock by 5, 10 or 20, depending on the setting of the EXPANSION FACTOR switch. In the X5 Mode, the 4 bit is fed back to the parallel load input of 6B. The counter then counts from 0 to 4 and resets to 0 in a continuous loop. As a result, the 4 bit is high for 1 μs out of 5, and the counter divides by 5. In X10 and X20, the counter, which is a decimal counter, simply counts through from 0 to 9 continuously. The top count output is high 1 μs out of 10. The top count output also toggles 5B, dividing the clock down to 20.

8C, 7C, 6C and 5C form the DISPLAY CLOCK ENABLE tree. Each of the eight inputs on 8C represents a condition under which the display clock should be allowed to count.

13A, 14A and 15A are the I/O control section. When COMMAND goes low, 15A is released from the reset condition. A high is clocked through both halves by the 1 MHz clock. The difference between the two halves generates a DUMP PRESET signal that becomes the PRESET B signal. The display section then goes through a normal PRESET cycle, with the exception that the PRESET time is only four counts long at the end of this cycle and the instrument will be in DUMP mode waiting for REQUEST. When REQUEST goes low, 13A will load a 13 (1101) into its parallel inputs, and TC will go low, allowing the counter to count. The 2 bit (Q1) will go high on the next 1 MHz clock, and Q0 will go low. This will generate a low on 16A-11. On the following 1 MHz clock, Q0 will go high and 16A-11 will go high. This 1 μs wide "low" on 16A-11 is a display clock enable that allows the memory to advance one location each time. At this time, TC will also go high and disable the counter. TC is also used as the FLAG output to indicate that valid data is present on the I/O lines.

If REQUEST is held low continuously, TC going high will parallel load 13A and the cycle will repeat itself until address 1020 is reached. The master reset input will be forced low and the counter will stop. Under this condition, data transfer will stop and COMMAND must first go high again before data transfer can resume.

If COMMAND is held low, and the instrument is ARMed after every complete data dump, the unit will take a new record, then immediately enter into the DUMP condition at the end of the record without going through a display cycle.

9C, 11C and 13C are a countdown counter used to generate the trigger marker. The PRETRIGGER DELAY set on the front panel LED display is latched into 10C, 12C and 14C. When DISPLAY CLOCK ENABLE goes high after PRESET time, the counters count down to 000. At this point the next word of data to be displayed will be the trigger word. The first half of 6A is clocked by this occurrence. The next enabled display clock will clock the second half of 6A. The difference between the two generates a one-memory-cell-wide pulse. This is the TRIGGER MARKER.

3C is the DISPLAY SEQUENCER. It selects the channel being displayed and establishes its DC level in the Y output amplifier. It counts each time the display goes into BLANK. The display sequence is as shown in Table 4.1.

When the counter counts from 8 to 9, PE on the counter goes low and 1 us later the counter is reloaded to 0000 and the sequence repeats. Each time 3C rolls from 9 to 0, 15B is allowed to count once. When the count is 15B reaches 15 (1111), TC goes high and forces PE low. 1 μs later, the counter is back to 0, and TC is low again. This 1 μs wide pulse on TC of 15B is ANDed with AUTO ARM (switch) and AUTO ARM ENABLE to produce the AUTO ARM pulse.

Table 4.1 Display Sequence

$\overline{\text{BLANK}}$	Q3	3C Q2	Q1	Q0	COUNT	CHANNEL SELECTED	DISPLAY
0	0	0	0	0	0	9	BLANKED, PRESET TIME and COUNTING to cursor position (if in EXPAND)
1	0	0	0	0	0	9	Data, No offset
0	0	0	0	1	1	8	BLANKED
1	0	0	0	1	1	8	Data, offset by 0.09 V
0	0	0	1	0	2	7	BLANKED
1	0	0	1	0	2	7	Data, offset by 0.18 V
0	0	0	1	1	3	6	BLANKED
1	0	0	1	1	3	6	Data, offset by 0.27 V
0	0	1	0	0	4	5	BLANKED
1	0	1	0	0	4	5	Data, offset by 0.36 V
0	0	1	0	1	5	4	BLANKED
1	0	1	0	1	5	4	Data, offset by 0.45 V
0	0	1	1	0	6	3	BLANKED
1	0	1	1	0	6	3	Data, offset by 0.54 V
0	0	1	1	1	7	2	BLANKED
1	0	1	1	1	7	2	Data, offset by 0.63 V
0	1	0	0	0	8	1	BLANKED
1	1	0	0	0	8	1	Data, offset by 0.72 V

Data from the memory is fed to the Y DAC through a level translator that changes the TTL signals to CMOS levels and a holding flip flop.

The Y DAC consists of R10, R11, R12, R14, R19, R22, R40, R41 and R42 (all inputs to a summing junction), amplifier 1B, driver transistor Q3 and feedback resistors R20 and R21. R16 provides damping of any potential ringing on the output cable. R21 provides adjustment of the output voltage amplitude. The output voltage is determined by the sum of currents into the summing junction.

The X ramp is generated by amplifier 1B and driver transistor Q1 charging C3. Q2 discharges C3 at the appropriate time. The voltage at 1B-1 is determined by the current through R8 and R9. This determines the amplitude of the ramp. The ramp provides a 1 ms sweep, with a 1 ms blanked time between sweeps.

4.3.3 Main Board

4.3.3.1 Input Buffer/Comparators

There are twelve front panel signal inputs on the 9100-D, as well as nine data inputs, two qualifiers and one clock. All input buffer/comparator circuits are identical.

The input signal is fed in through the input BNC and is offset by the threshold voltage through R1 and R2, such that when the input signal is at the desired threshold the input gate is at 0 V. The FET is used as a source follower, so the input signal now appears at the source (and one input of the 10216) offset by the V_{GS} of the FET.

The other FET is used to provide a reference for the other 10216 input. If both FETs were perfectly matched, the second gate would be at ground. Since there is some difference in V_{GS}, the second gate is brought to a pot to allow it to be shifted about ground. This compensates for the difference in V_{GS}.

The 10216 is an ECL line driver/receiver. It is used as a comparator. Each section has a gain of approximately 5. R216 is a hysteresis resistor, which provides approximately 10 mV bysteresis. When the input signal goes above threshold, the 10216 signal input will rise above the reference input. This will be amplified through the stages of the 10216 to produce ECL output signals that switch whenever the input signal crosses threshold.

4.3.3.2 Latch/Glitch Catching

A typical latch/glitch catching circuit (such as is used on input 1) consists of two flip flops (13M and 14M) and two gates (15M). When pin 9 of 14M is high (15M-9 is low), the last data level is held on 14M-15 and gates 15M are enabled. 13M-15 will also maintain the same data level as 13M-15 (data is clocked from 13M-15 into 14M). When a data level different from the current state appears on 18M-6 and -7, 14M is either set or reset through gates 15M (depending on current state and new data level). This new level is then passed onto 13M on the next clock. This also resets or sets 14M (opposite action from above) if the change was momentary (a glitch). Otherwise data gets transferred to 13M on every clock.

When 14M-9 is low (15M-9 is high), gates 15M are disabled and any data present at 14M-10 will appear on 14M-15 and get clocked into 13M on the next clock. This data will have to be present at least one full clock period to be detected.

4.3.3.3 Combinational Trigger

The combinational trigger circuit consists of a 10121 (16M in channel 1), 13H(10176) and 12H (10231). The 10121 will output a low level signal when the selected condition for the given channel is met. This level is latched into 13H. The outputs of 13H are wire-ORed together, forming the TRIGGER NODE. The EXTERNAL TRIGGER IN signal is also wired into the node, allowing expansion of triggering to include external trigger sources.

12H resyncs the TRIGGER NODE and detects the edges of the signal on the node. 12F is the trigger selection tree, which selects either external or internal trigger and

the true or false edge of the internal trigger.

4.3.3.4 Arm Logic

16D is the arm select tree. It allows selection of internal or external arm and manual (single) or automatic (repetitive) arm.

4.3.3.5 Record Control Logic

The record control logic section consists of the ARM and TRIGGER flip flops (14F), the RECORD flip flop (14E) and the PRETRIGGER HOLDOFF and DELAY INHIBIT flip flops (16E).

The ARM flip flop senses the presence of an arm signal and flips. This releases the reset inputs on the RECORD and TRIGGER flip flops. If the unit is in PRETRIGGER or EVENTS DELAY mode, a signal is generated through 18D to set the RECORD flip flop. One sample clock later the second half of 14E flips, removing the signal from 18D. The TRIGGER HOLDOFF flip flop holds the $\overline{J}$ input to the TRIGGER flip flop high, preventing any triggers from being sensed. At the end of one full record cycle through memory, the PRETRIGGER HOLDOFF flip flop is clocked and releases the $\overline{J}$ input of the TRIGGER flip flop, allowing it to accept triggers.

In the CLOCK DELAY mode, when 14F senses the arm signal and flips, the resets on the RECORD and TRIGGER flip flops are released, enabling them to accept triggers. When the TRIGGER flip flop sees a trigger event, it flips and one clock later the RECORD flip flop flips.

When the TRIGGER flip flop sees a trigger event and flips, it enables the DELAY COUNTER. In PRETRIGGER mode, the delay counter is loaded with the amount of delay desired. When the counter is enabled, it will count until it reaches 1020. 14D is used to decode this condition and generates a low level at the $\overline{K}$ inputs of 14E and 14F. At the next clock edge, the flip flops sense this level and change state, taking the instrument out of the RECORD condition and disabling the counter. In CLOCK DELAY, the delay inhibit circuit (16E) is enabled, and the counter (which is loaded with the nine's complement of the delay desired) must first count up to 9999. This condition is detected by 18D and is fed into 16E as a clock input, latching the level on the output of 16E. This disables 15E and enables the 1024 decoder. When the counter reaches 1024, it presents a low level at the $\overline{K}$ inputs of 14E and 14F. The flip flops change state and recording stops.

In EVENTS DELAY, the unit begins recording as soon as it is armed (as in PRETRIGGER), and will not accept triggers until the PRETRIGGER HOLDOFF time is completed. The DELAY INHIBIT circuit is also enabled, and the nine's complement of the delay desired is loaded into the delay counter. 15E is enabled, holding the counters off. Each event allows the counter to count once, until 9999 is reached. The DELAY INHIBIT circuit is then clocked, and the counter is allowed to count to 1020, at which time the unit recording stops.

Figure 4.4 is a graphic representation of the sequence of events.

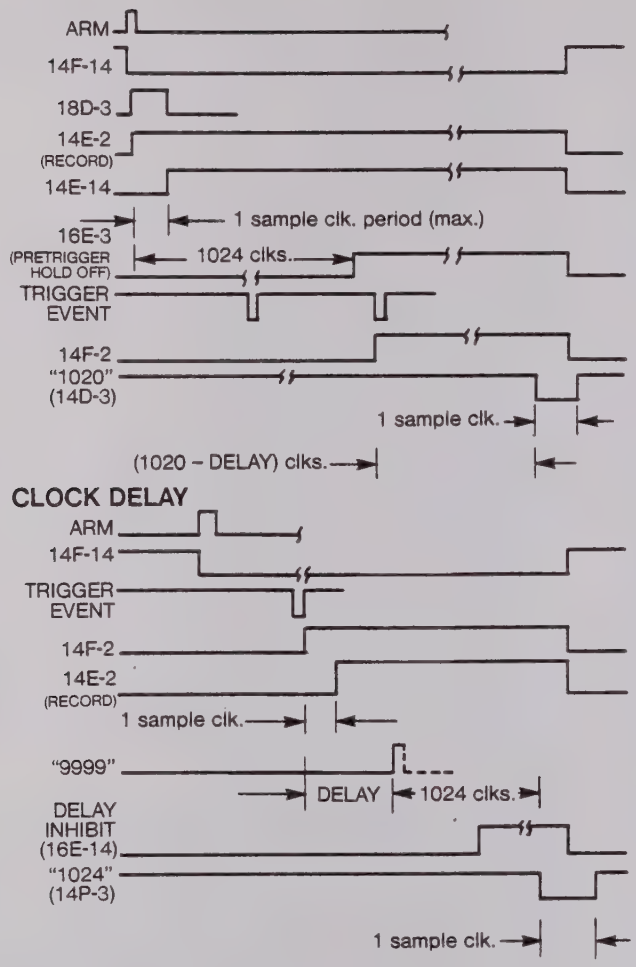
4.3.3.6 Memory Control Logic

Gates 15D enables the memory address counter whenever the memory needs to be advanced, either in record or in display. 12D selects the appropriate memory clock frequency.

4D, 2D and 1D are the memory address counter, 4D is a 4-bit shift register that shifts one pulse through it, generating a four-phase clock. 2D and 1D are cascaded 4-bit hexadecimal counters that generate the memory address.

4C, 2C and 1C are the memory address save register. The last address recorded into is saved in this register to serve as a reference point for starting the memory during the display cycle.

E6, E8, D6 and D8 are identical circuits that generate the $\overline{\text{WRITE ENABLE}}$ pulses for the memory from the four-phase clock generated by 4D. The $\overline{\text{WRITE ENABLE}}$ pulses are approximately 20 ns wide and start



NOTE: IN EVENTS DELAY a total of N + 1 events is required to complete the delay cycle, 0 delay requires 1 event, 1 delay requires 2 events, etc.

Figure 4.4 Sequence of Events

approximately 20 ns after a clock.

Figure 4.5 shows the relationship of the four-phase clock and WRITE ENABLES.

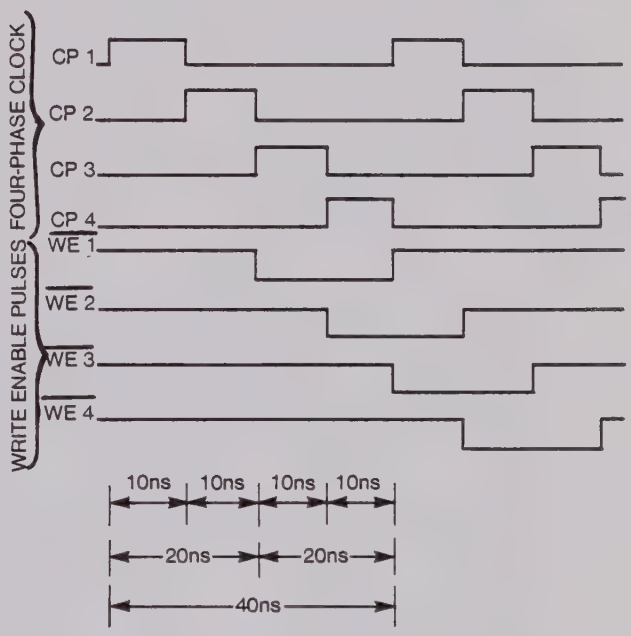


Figure 4.5 Four-Phase Clock and WRITE ENABLE Pulses at 100 MHz Record Rate

All the ECL signals (data and clocks) go through level translator devices (10125s) for translation to TTL level signals. This is required because the main memory is composed of TTL RAMS.

4.3.3.7 Memory

The memory is a 1024 X 9 static RAM system. Each channel is composed of four 256 X 1 static RAMs running at 25 MHz. Each RAM is clocked by one of four phases of the address clock, producing an effective 100 MHz maximum rate.

1B, 2B and 3B are the output data select logic. Data from one of the nine channels is selected for presentation of the display generation logic on the control board. The control signals for the selection logic are generated by the display sequence on the control board.

4.3.4 ECL Prememory Board

The ECL prememory board consists of four sets of data latches and level translators. The data latches are clocked by the four-phase clock generated by 4D on the main board, producing an effective 100 MHz maximum clock rate.

The level translators change the ECL level data to TTL level data.

4.3.5 Power Supply

The power supply is a series pass type and has foldback current limiting and overvoltage crowbar protection. The circuit will maintain regulation with only a 0.6 V drop from input to output, thus enabling the supply to achieve good efficiency. Figure 4.6 is a simple block diagram of the regulator circuit. The negative regulator is very similar to the positive regulator and is connected so that the negative output tracks the positive output. There are two adjustments for the output voltages. The positive output is adjusted by potentiometer R37, and the ratio of the negative output to the positive output is adjusted by potentiometer R49.

Figure 4.7 is a simplified schematic of the positive regulator circuit. The configuration of the pass transistor Q2 and the driver transistor Q5 is especially chosen to allow operation with the minimum voltage drop from input to output. The resistor R18 is necessary to limit the base current to Q2 during turn on and in case of very low input voltage. A Darlington transistor is used for Q5 to provide sufficient current gain to drive the pass transistor into saturation at a 5-A output. The pass transistors are mounted to a heat sink directly in front of the fan and are electrically insulated from the heat sink. The driver transistors are mounted on a small heat sink on the printed circuit board and are also insulated.

The reference voltage circuit consists of two op amps and a monolithic dual diode. Refer to Figure 4.8. The dual diode CR9 provides a temperature stable reference in the following way. The reference voltage circuit makes use of the temperature tracking of the two diodes and, by setting the current level in each diode properly, achieves a cancellation of the temperature coefficients of the two diodes.

To provide reference stability with respect to input voltage changes, a current source is formed by the op amp U1-A and resistors R31, R32, and R40. This provides a constant 20 mA to diode "B." The reference voltage output as a function of input voltage is shown in Figure 4.9.

In normal operation, the op amp U1-C compares the reference voltage to the feed back voltage (from R44 and R43) and controls the driver transistor Q5 in such a way as to maintain the output voltage at the desired value. If the output is low, the op amp U1C will go more positive and cause Q5 to pull more current from the base of Q2, thus causing Q2 to provide more current to the output to raise the voltage. The resistor R9 provides current to the output to ensure startup.

The current limit circuit consists of op amp U1-D and resistors R10, R11, R21, R22, R41, R42, R47, R48, CR8, and CR13. The circuit acts as a differential comparator and when the voltage across R10 and R11 reaches the value determined by R21, the op amp will go positive and force the regulator to be controlled by the current limit circuit U1-D. The typical values of current limit are 7.5 A (375 mV) for +5 output and 9A (450 mV) for -5.2 output. The diode CR13 and resistor R48 introduce additional current to the network to increase the current allowed at low-output voltages. This ensures startup. The resistor R50 in the negative regulator performs this same function.

The overvoltage crowbar circuit of Q4, CR6, R23, and C6 are shown in Figure 4.10. The SCR Q4 will be triggered when the output voltage reaches CR6 plus the gate trigger voltage of Q4 (about 1 V). This value is typically 7.2 V. This circuit is intended to protect the system in case of a failure of one of the pass transistors. If Q2 fails, the output voltage will rise until it reaches about 7.2 V, at which time the SCR will be fired

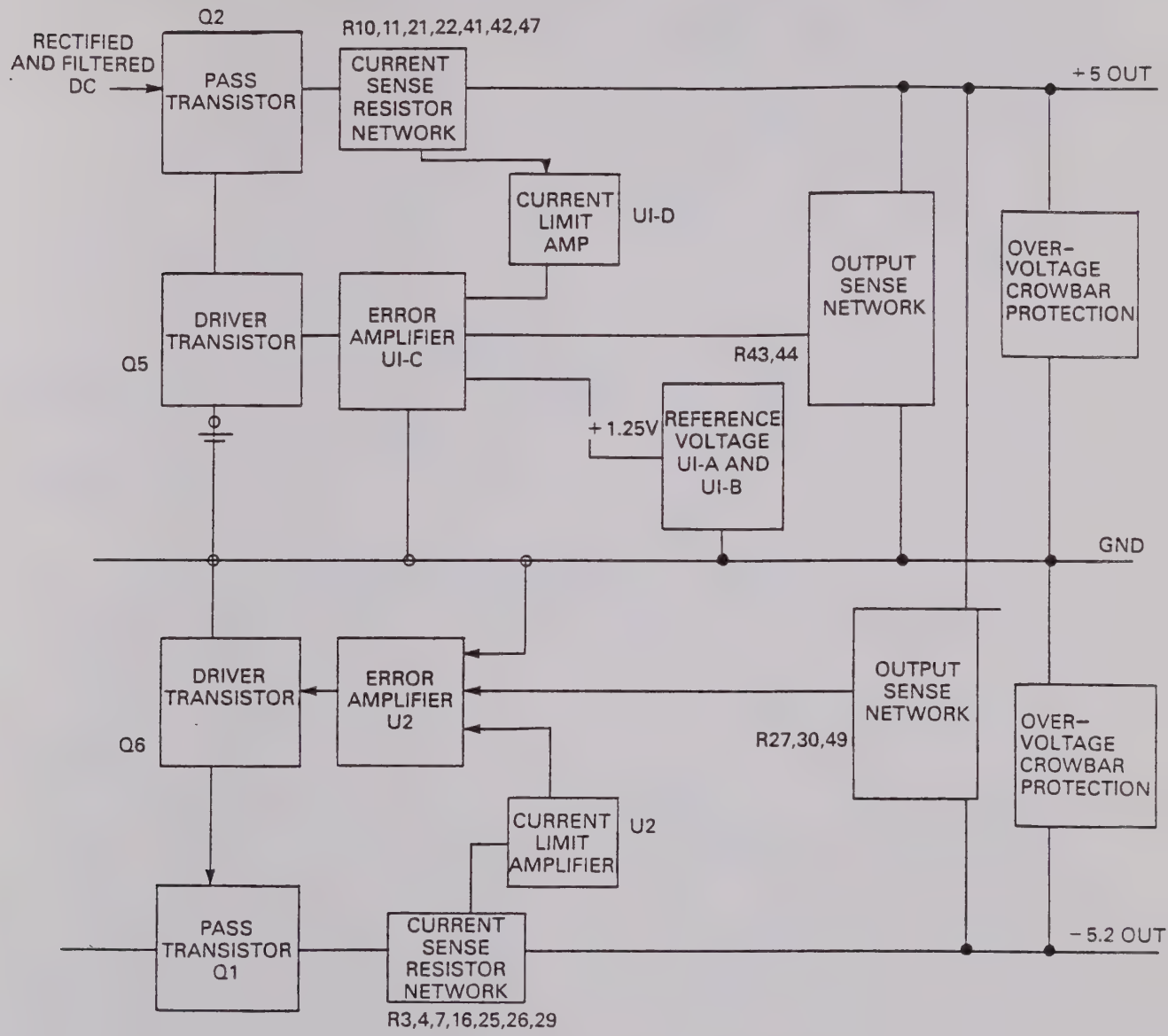


Figure 4.6 Power Supply Block Diagram

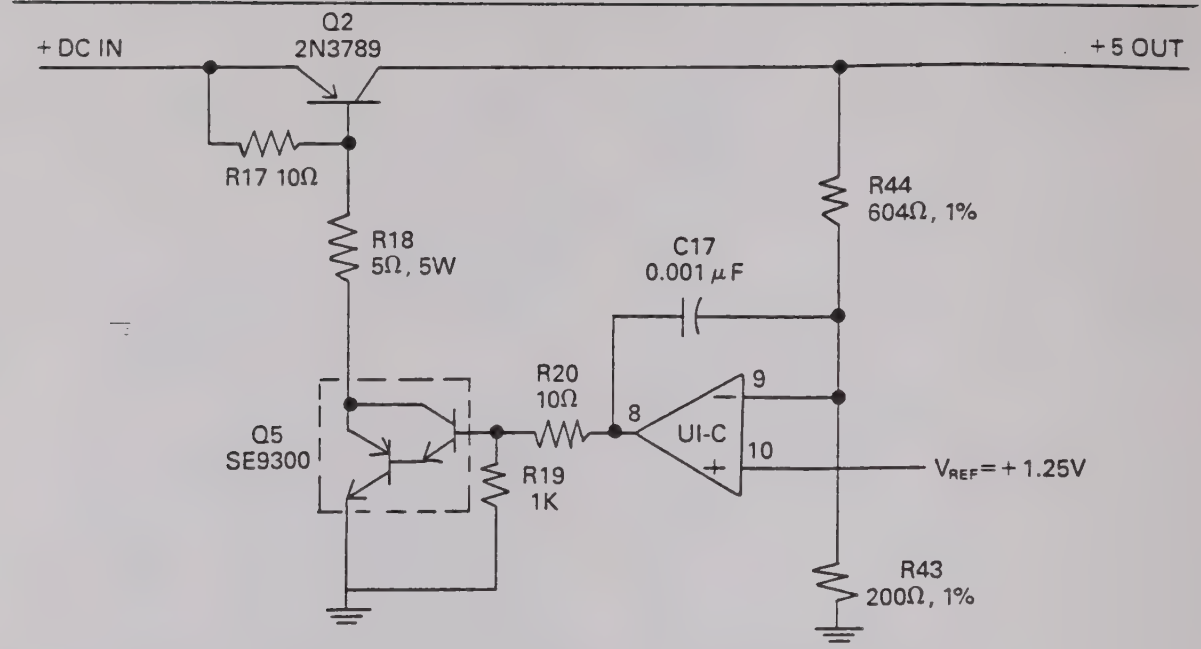


Figure 4.7 Simplified Schematic Positive Regulator

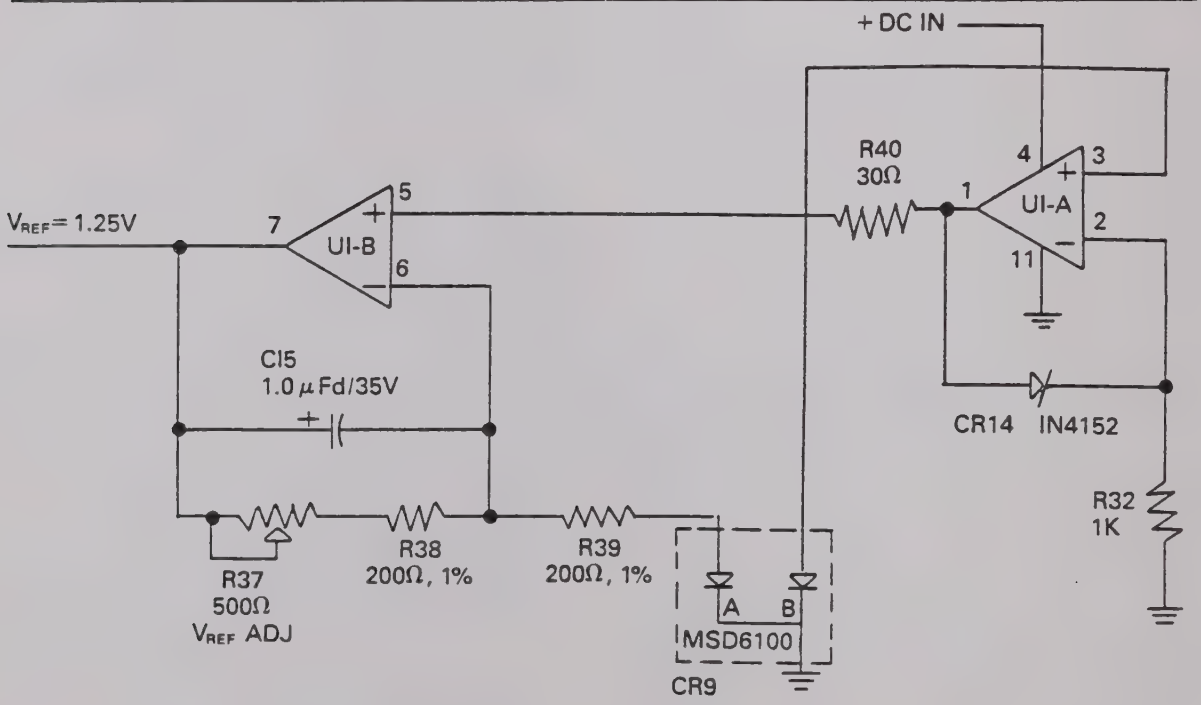


Figure 4.8 Schematic - Reference Voltage

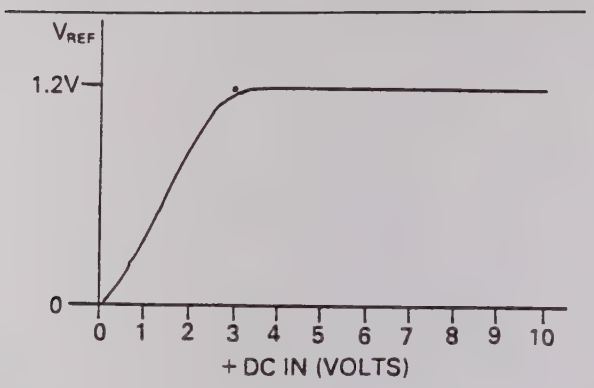


Figure 4.9 Reference Voltage Versus Input Voltage

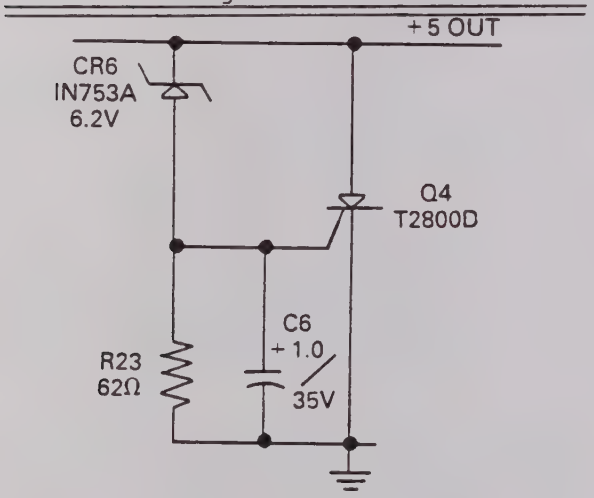


Figure 4.10 Overvoltage Crowbar Circuit

and draw the output voltage down to about 0.9 V. Because the transistor Q2 has failed as a short circuit, the current limiting circuit will not function and the current drawn by Q4 will be determined by R10, R11, and the wiring resistance. This will normally be a large current (> 10 A) and will cause the fuse to blow.

Provisions for selecting the nominal line voltage of 100, 120, 220 or 240 V is provided in the AC power-plug unit on the rear panel. Also included in the AC power-plug unit is an RFI filter. The transformer is specified for operation from 50 to 400-Hz line frequency.

The power supply includes provision for remote sensing of the output voltages to eliminate the effects for voltage drop in the connecting lines. Resistors R46, R28, and R35 are included to establish the sense voltage in the event that the remote sense lines become disconnected. In this case the output voltages will increases by about 0.1 V.

SECTION V

OUTPUT INTERFACE

5.1 Introduction

The output interface of the Model 9100-D includes two methods of analog output: one, using a CRT in an X-Y-Z mode, and two, using an oscilloscope in the triggered mode. These methods are explained in Section 3.4.

The instrument also offers a digital output of data. This data is output in a 9-bit parallel format, the bits representing a simultaneous data entry for all channels. One thousand twenty such 9-bit words are available in the digital output mode.

5.2 Digital Output

The inputs and outputs at the 24-pin rear panel connector are positive logic, TTL signals except for pin 5, which is the only CMOS (-voltage) signal. Direct access to control gates is available at the connector. This connector provides the physical interface for digital data output. The connector is an Amphenol Micro Ribbon 57-40240. The mating connector is an Amphenol part number 57-30240.

The pin assignment, and signal descriptions for the digital interface are listed in the following table:

Pin #	Signal Name	Description
20 18 19 16 17 22 23 24 21	Data Output 1 Data Output 2 Data Output 3 Data Output 4 Data Output 5 Data Output 6 Data Output 7 Data Output 8 Data Output 9	These lines supply data stored in memory when the digital output procedure, outlined in Section 5.2.1 or 5.2.2 below, is followed. Buffering is provided.
2	CMD (INPUT)	This line is internally pulled high. To initiate a digital output, pull to a TTL low level.
3	Request (INPUT)	This line is internally pulled high. Pulling to a TTL low level causes the unit to "fetch" the next data word.
4	Auto Arm Mode (OUTPUT)	This line is at a TTL high level when the instrument is in Auto Arm, otherwise it is at a TTL low level.
5	Auto Arm Enable	This line is normally at a CMOS high level (0 V). To stop re-arming, pull to a low level (-5 V).
6	1 MHz Clock (OUTPUT)	A TTL level that is high 0.6 μs and low 0.4 μs.

Pin #	Signal Name	Description
14	Flag (OUTPUT)	This line goes high when the next data word is available, approximately 2 µs after the request input is pulled low.
7	M>N (OUTPUT)	Synchronous with the display output at TTL levels, this line is low up to the cursor address and high after the cursor address.
12	Display (OUTPUT)	Low when the 9100-D is recording; high otherwise.
9	-5.2 VDC	
8	+5 VDC	
11	Trigger (INPUT)	The Trigger Input must be brought to a TTL high level to trigger the analyzer.
10	Remote Arm (INPUT)	This input is normally held low and brought high to arm the unit.
1, 13	Ground	Power and logic return.

5.2.1 Digital Output Sequence - After Display

Immediately after recording, the 9100-D will enter the display mode, repetitively cycling the memory and producing the X, Y, and Z display signals. In this condition, the Display (pin 12) output signal will be high. The Command (pin 2) input is pulled high by an internal pull-up resistor (1K to +5 V).

To initiate an output transfer, the "COMMAND" input should be brought low and held low until the desired memory transfer has been completed. As long as the COMMAND input is held low and the Display output is High, the 9100-D will be in the DIGITAL OUTPUT mode. A new recording may be initiated at any time by the record control logic and will immediately terminate the Digital Output mode.

When in the Digital Output mode, data may be transferred in two ways; continuous transfer or single byte.

5.2.1.1 Single Byte Transfer

Each byte is initiated by presenting a REQUEST pulse (minimum 1 µs, maximum 20 µs) on pin 3. The 9100-D will assemble the 9 data bits of the currently addressed memory word and will indicate when the data is ready by bringing FLAG output high. The data will be stable at least 50 ns before the Flag goes high.

The next, and subsequent data words will be presented on the data output lines after each Request (pin 3) Input low level. For proper data output the interval between REQUEST inputs should be no closer than 5 µs giving asynchronous data rates 200K bytes/s to DC.

5.2.1.2 Continuous Transfer

Continuous data transfer will be performed if the Request line is held low. The Request line may be held low before Command is brought low. Each time a data byte is ready, the Flag line will be brought high for 1 µs. The data will be stable 50 ns before the FLAG goes high and will remain stable 500 ns after the Flag goes low. The data rate will be 3 µs per byte.

5.2.2 Digital Output Sequence - After Record

If it is desired to output digital data immediately after Record, proceed as follows: Hold Command (pin 2) low. As soon as Record is complete (Display goes high), the first data word can be read. When this occurs, proceed with data transfer operation as described above. When the desired memory length has been transferred, return the Command Input (pin 2) high for further record sweeps.

NOTE: The memory of the 9100-D contains 9 X 1024 bits. Only the first through 1020 bits of each channel memory are specified to be valid output data.

CAUTION: If the ARM IN and/or TRIG IN BNC connectors on the rear panel are enabled, Remote Arm (pin 11) and Trigger (pin 10) must be left floating (high).

SECTION VI

CALIBRATION

6.1 Introduction

The following calibration procedures are intended to be used for recalibration of the internal circuits of the 9100-D. The instrument was completely calibrated before shipment and should not need recalibration for at least six months or 1000 hours of operation. See Table 6.1 for the required test equipment.

Table 6.1 Required Test Equipment

Type of Equipment	Name of Manufacturer
Oscilloscope	Tektronix 475 or equivalent
Digital Voltmeter	Dana 4200 or equivalent
Pulse Generator	Tektronix PG502 or equivalent
Universal Counter/ Timer	Tektronix DC 505 A or equivalent

NOTE: Allow a 20 minute warm-up period before calibrating the 9100-D.

For all DC measurements, use any front panel BNC as ground for the voltmeter.

6.2 Display Output Adjustments

Monitor X OUT BNC with oscilloscope.

Adjust R9 for a 1.0 V p-p signal.

Monitor Y OUT BNC with oscilloscope.

Adjust R21 for a 0.8 V p-p signal.

Refer to Figure 6.1 for the locations of adjustment for the Control Board Assembly.

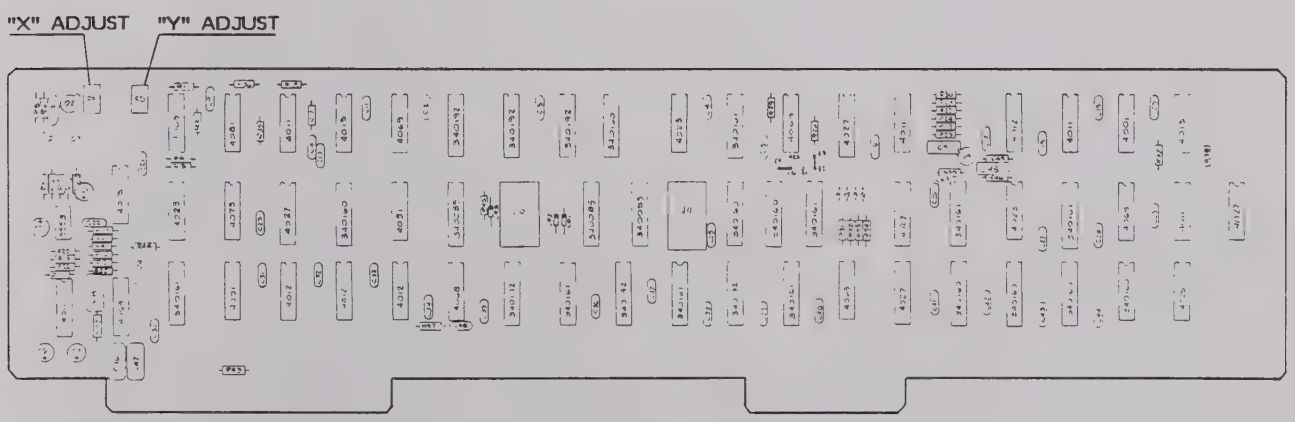


Figure 6.1 Control Board Assembly

6.3 Power Supply Adjustment

1. Both power supply voltages will be measured on the main board near the power connector. The +5 V should be read on the bus bar. The -5.3 V reading should be taken from the large trace next to the bus bar.

2. The +5 V supply should read +5.00 VDC ±0.01 VDC. Adjust R37 on power supply regulator board to obtain the correct measurement. Refer to Figure 6.2.

3. The -5.3 V supply should read -5.30 VDC ±0.01 VDC. Adjust R49 on power supply regulator board to obtain the correct measurement. Refer to Figure 6.2.

6.4 Threshold Level Calibration

Select channel 1-4 and 5-CLK thresholds to TTL X1. Connect voltmeter to test point 1-4. Adjust the TTL resistor on the front panel PC board for a reading of +1.40 VDC ±0.02 VDC. Check the channel 5-CLK test point for the same reading. Change both channel 1-4 and 5-CLK thresholds to TTL X10. The readings of the test points should stay the **same** as the TTL X1 readings.

NOTE: For increased accuracy, keep both threshold knobs in TTL X10, and measure 1C M20 pins 1 and 7. The readings should be -73.7 mVDC ±3.5 mVDC.

Repeat this procedure for the ECL and VAR thresholds. Refer to Table 6.2 for specifications. See Figure 6.3 for the locations of adjustment.

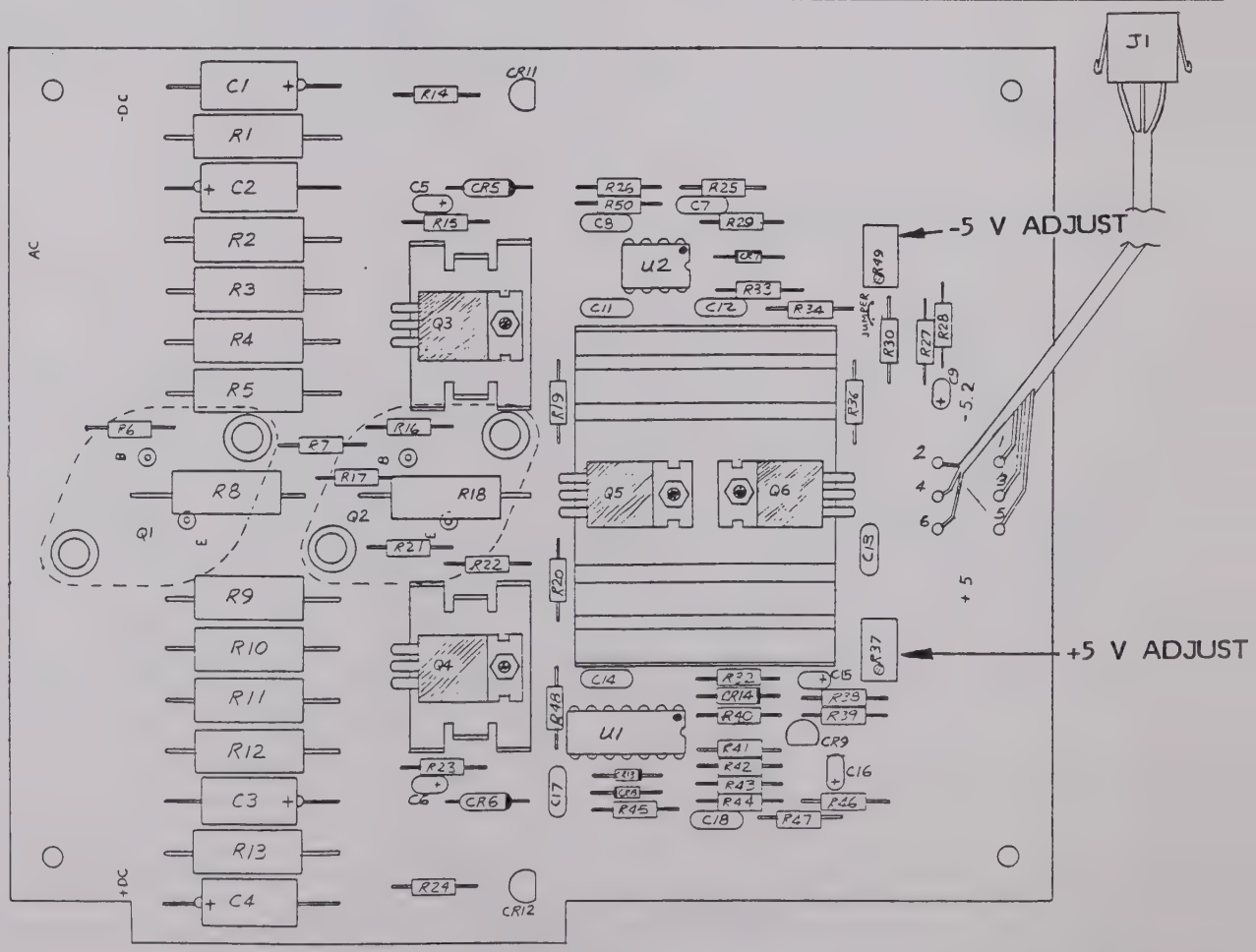
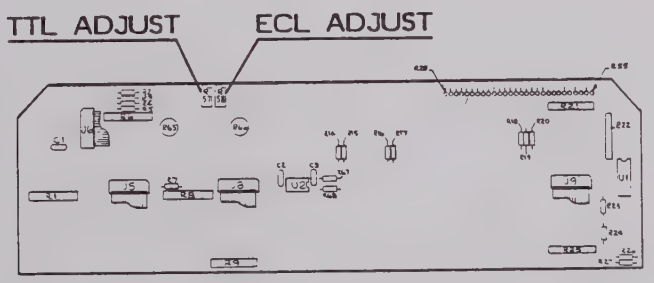


Figure 6.2 Power Supply Regulator Board Assembly

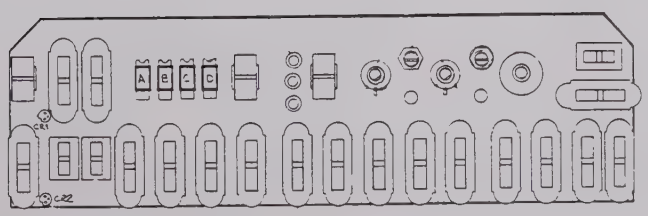
Table 6.2 Threshold Level Specifications

	CH 1-4 TEST POINT	CH 5-CLK TEST POINT	IC M20 PINS 1 and 7
TTL X1	+1.40 ±0.02 VDC	+1.40 ±0.02 VDC	
TTL X10	same	same	-73.7 ±3.5 mVDC
ECL X1	-1.30 ±0.02 VDC	-1.30 ±0.02 VDC	
ECL X10	same	same	+68.4 ±3.5 mVDC
VAR X1	±2.75 ±0.25 VDC	±2.75 ±0.25 VDC	
VAR X10	same	same	-131.6 ±3.5 mVDC*

*Set thresholds to VAR X1. Adjust front panel potentiometers to +2.50 VDC. Change thresholds to VAR X10 and take readings.



COMPONENT SIDE



SOLDER SIDE

Figure 6.3 Front Panel PC Board (Component Side)

6.5 Input Bias Adjustment

Refer to Figure 6.4 for the locations of adjustment on the main board assembly.

Ground the front panel threshold test points. Select channel 1-4 threshold to VARIABLE X10. Connect the voltmeter to IC 20M-7. Adjust R119 for a reading of 0.0 mVDC. Change channel 1-4 threshold to VARIABLE X1. The voltmeter reading should not change more than 15 mVDC.

IC 20M-7

VARIABLE X10 should be 0.0 mVDC ±0.1 mVDC.

VARIABLE X1 should be 0.0 mVDC ±15 mVDC.

Repeat this procedure using IC 20M-1 as the test point and channel 5-CLK threshold. Adjust R120 for correct voltages.

IC 20M-1

VARIABLE X10 should be 0.0 mVDC ±0.1 mVDC.

VARIABLE X1 should be 0.0 mVDC ±15 mVDC.

With the threshold test points still grounded, input a 10 mV p-p square wave (symmetrical around ground) into the channel 1 BNC (use a Biomation X10 probe). Sync the oscilloscope to the pulse generator trigger output. Connect the oscilloscope to the channel 1 twisted pair (either wire) as designated on the main board. Adjust R5 until a symmetrical square wave appears on the oscilloscope.

Repeat this procedure for all of the front panel inputs, using the appropriate twisted pair and resistors. When all adjustments have been completed, remove ground from threshold test points.

6.6 Memory Write Enable to Clock Set up

NOTE: To perform these adjustments, the power supply must be removed from the chassis.

Set all combinational trigger switches to "X". Select a time base of 0.01 µs, Arm to Single and Record to Pretrigger. Manually arm the unit; display should blank.

Connect channel 1 of the oscilloscope to TP1 (3E-4), channel 2 to TP2 (11E-5). Sync the oscilloscope to the rising edge of the channel 1 signal. Adjust R101 until the falling edge of the channel 2 signal is 20 ns behind the rising edge of the channel 1 signal. Adjust R100 until the rising edge of the channel 2 signal is exactly on the rising edge of the channel 1 signal. See Figure 6.5.

Perform the preceding procedure with the following test points and resistors in Table 6.3. Refer to Figure 6.4 for locations of adjustment.

Table 6.3 Test Point and Resistor Set Up

TP1	TP2	Resistors
3E-4	11E-5	R101 and R100
3E-5	11E-13	R105 and R104
3D-5	11E-12	R99 and R98
3D-4	11E-4	R103 and R102

6.7 Internal Clock Adjustments

Connect the universal counter to the CLK OUT BNC on the rear panel. Select internal time base of 0.01 µs. Adjust capacitor C22 for a reading of 99.99 MHz. Select an internal time base of 0.02 µs. Counter should read 49.99 MHz. Power down unit, wait 5 seconds and power it back up. Counter should be locked on a reading of 49.99 MHz. If not, readjust C22 and perform the power down, power up check again.

6.8 Probe Calibration

The Model 9100-D has a Probe Compensation Test Point that allows a Biomation X10 probe to be monitored while the probe is compensated to the unit's input characteristics.

1. Connect an oscilloscope with its compensated probe to the Probe Compensation Test Point on the front panel of the 9100-D.

2. Connect the Biomation X10 probe to be compensated to the EXT CLK BNC.

3. Connect an external pulse generator (with a 1 kHz square wave output at 0 V to +5 V levels) to the input of the probe under test.

4. Monitor the signal on the oscilloscope while adjusting the trim capacitor in the Biomation X10 probe for best looking square wave.

5. The probe is now ready to be used with the logic analyzer.

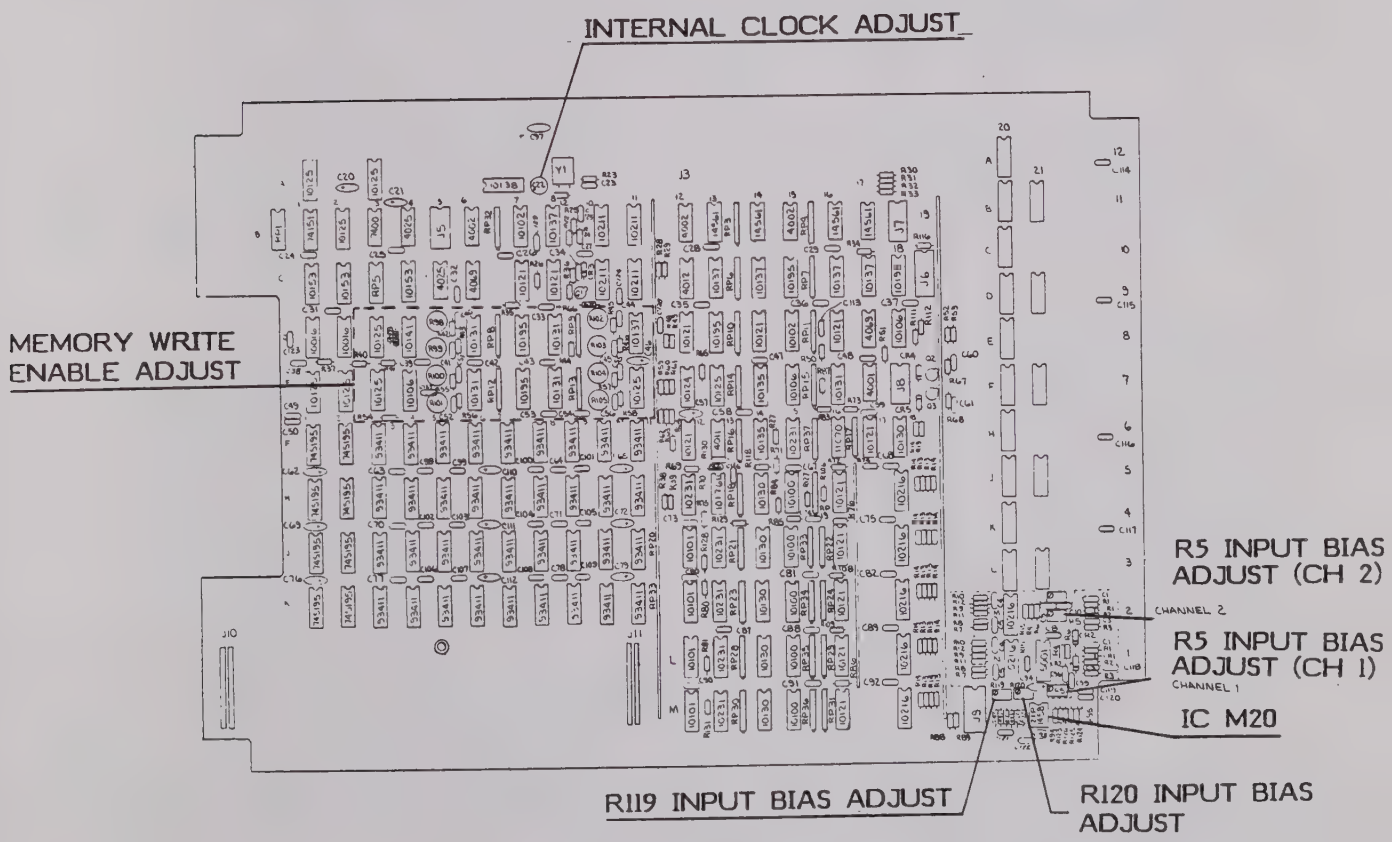

INTERNAL CLOCK ADJUST
MEMORY WRITE ENABLE ADJUST
R5 INPUT BIAS ADJUST (CH 2)
R5 INPUT BIAS ADJUST (CH 1)
IC M20
R119 INPUT BIAS ADJUST
R120 INPUT BIAS ADJUST

Figure 6.4 Main Board Assembly

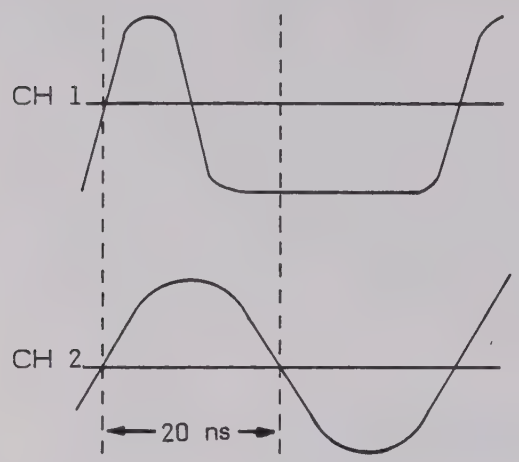


Figure 6.5

SECTION VII

MAINTENANCE

7.1 Introduction

This section covers the maintenance procedures for troubleshooting and repair of the Model 9100-D. Additional assistance in a particular problem can be obtained by contacting the Customer Service Department at the factory: Phone (408) 988-6800, TWX (910) 338-0509.

7.2 Initial Setup

Power up the 9100-D and allow it to warm-up for 20 minutes. Check the Control board for jumpers P2, P3, and P4 at location 17B. These jumpers must be in for smooth display movement.

Set front panel controls as follows:

Arm - Auto
Record - Pretrigger
Delay/Cursor - Delay
Threshold Channel 1-4 - TTL X10
Threshold Channel 5-CLK - TTL X10
Internal Clock - 0.01 μs
Horizontal - X1
Trigger Source - Internal True
Combinational Trigger, Channel 1 - "1", Channel 2-9, TQ and CQ -"X"
Clock Source - Internal

Input a 1 MHz TTL square wave (0 to 2.5 V) into channels 1-9 using Biomation X10 probes. Make sure probes have been properly compensated. This input will be used for the following tests.

7.3 Clock

7.3.1 Clock Out

Connect the oscilloscope to the CLOCK OUT BNC on the rear panel. The signal shown on the oscilloscope should have the same period as that selected by the INTERNAL CLOCK control on the front panel. One at a time, select all of the time base settings and verify that the CLK OUT BNC has the same frequency as the control indicates. Return the internal clock to 0.01 us.

7.3.2 Internal Clock

Adjust input signal for 100 kHz. Data displayed should be one complete cycle. Change time base to 0.02 μs. Display should show two complete cycles. Change time base to 0.05 μs. Display should show five complete cycles.

Divide input signal by a factor of 10 (10 kHz) and verify that the 1, 2, 5 pattern repeats itself for the next three time bases. Check all time bases, dividing input signal by 10 for each 1, 2, 5 sequence.

Return to the fastest time base one step at a time. At each step, vary the input signal so that from five to ten cycles are displayed. The display should show clean square waves without any breaks or dropped bits. When completed, the internal clock should be at 0.01 us. Set HORIZONTAL to EXPAND, HORIZONTAL EXPAND to X20; increase input signal until data begins to break up. Verify that good data is displayed up to at least 30 MHz.

Adjust input signal for one cycle at X1 expansion.

7.3.3 External Clock In

Using a second pulse generator and a Biomation X10 probe, input a 10 MHz TTL square wave (0 to 5 V) into the EXT CLK input on the front panel. Set CLOCK SOURCE to EXT⌝⌞. The display should show ten times as many pulses on it. Increase the clock frequency until the data begins to break up, then reduce the frequency until there is good data again. Now measure the frequency of the clock signal. Minimum acceptable frequency is 70 MHz.

Set CLOCK SOURCE to EXT⌟⌜. Repeat the above procedure for the positive-going

clock edge.

Slowly decrease the clock frequency and data frequency as required. Check the display for a clean waveform throughout the full range of the external clock. Return to INTERNAL CLOCK. Remove external clock signal.

7.3.4 Clock Qualifier

Select a time base of 0.02 µs. Adjust the data input frequency until three square waves are visible on the display. Adjust the data input pulse width until the positive-going pulse is two-fifths (40%) of the signal period. See Figure 7.1. Move the channel 9 input to the clock qualifier input.

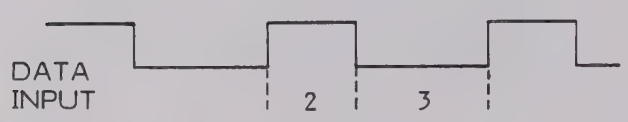


Figure 7.1 Data Input Pulse Width

Set CLOCK QUALIFIER to "0". The display should show approximately four or five positive pulses one or two clocks wide.

Set CLOCK QUALIFIER to "1". The display should show approximately six or seven negative pulses one or two clocks wide.

Set CLOCK QUALIFIER to "X". Move clock qualifier input back to channel 9 input. Return internal clock to 0.01 µs.

7.4 Arm

Set ARM to SINGLE. Manually arm the unit and verify that new data is being recorded.

Set ARM to EXTERNAL. The display should go blank. Input a 100 Hz pulse approximately 10 ns wide at 1.9 V amplitude into the ARM IN BNC on the rear panel. The 9100-D should show a flickering display. Remove the ARM IN signal.

Set ARM to AUTO. Connect the oscilloscope to the ARM OUT BNC on the rear panel. Hold the MANUAL ARM switch down. The scope should show a 300-400 ns wide positive-going pulse.

7.5 Trigger

7.5.1 Trigger - True and False

Set combinational trigger for channel 1 to "X". Manually arm and trigger the 9100-D several times. The unit should show an asynchronous trigger display. Set combinational trigger for channel 1 to "1" with TRIGGER SOURCE still in INT (T). The display should show the first level of data as high and the first transition as negative going. Set the combinational trigger for channel 1 to "0". The display should show the first level of data as low and the first transition as positive going. Set TRIGGER SOURCE to INT (F). The display should show the first level of data as high and the first transition as negative going.

Connect the oscilloscope to the rear panel TRIG OUT BNC. The signal on the scope should be the same as the data going into channel 1.

Return TRIGGER SOURCE to INT (T) and channel 1 combinational trigger to "1".

7.5.2 External Trigger

Set TRIGGER SOURCE to EXT. Change channel 1 combinational trigger to "X". The 9100-D should show a rolling, asynchronous display.

Trigger a second pulse generator off of the data input pulse generator. Adjust the output of the second pulse generator for a 10-ns wide pulse with an amplitude of 1.9 V peak. Connect this signal to the TRIG IN 1 input on the rear panel. The unit should now have a stable synchronous display. Move the trigger signal to TRIG IN 2. The 9100-D should still have a stable synchronous display.

Set TRIGGER SOURCE to INT (T) and disconnect the rear panel trigger input signal.

7.5.3 Combinational Trigger

Remove the inputs to channels 2-9, leaving an input signal to channel 1 only.

Set channel 1 COMBINATIONAL TRIGGER to "1". The display should show a high level at the beginning of the display and the first transition should be negative.

Set channel 1 COMBINATIONAL TRIGGER to "X". The display should blank.

Set channel 1 COMBINATIONAL TRIGGER to "0". The display should show a low level at the beginning of the display and the first transition should be positive.

Repeat this procedure using channels 2-9 and TQ. Be sure to input a signal only to the channel being tested, with the exception of TQ. To test the combinational trigger for TQ, leave a signal in the channel 9 BNC with the COMBINATIONAL TRIGGER in "X". Input another signal into the TQ BNC and perform the test.

Return channel 1 combinational trigger to "1" and all other inputs to "X". Reconnect signals to channels 1-9.

7.6 Horizontal

Set DELAY/CURSOR display to CURSOR and ARM to SINGLE. Arm and trigger unit. Increment the cursor to 150. Set HORIZONTAL to MIX. The 9100-D should show a X1 expansion from the left edge of the display to the cursor position. From the cursor position to the right edge of the display, the display should show an expansion of X5. Increment cursor to 200. The display should not jitter and the cursor should move slower than in X1.

Set HORIZONTAL to EXPAND. The entire display should be expanded X5. Decrement cursor to 150. The display should not jitter as data moves across the display.

Select expand X10 and then X20. Each time the display should expand by the factor selected.

Select HORIZONTAL to X1, HORIZ EXPAND to X5, and ARM to AUTO.

Decrement cursor to 000.

7.7 Memory Check

Set the INTERNAL CLOCK to 2 ms. Input a 80 Hz square wave at 1.9 V peak amplitude. The display should show a high number of data transitions without losing its square wave recognition.

Set ARM to SINGLE. Manually arm the unit. The display should show no extra data points or data transitions.

Repeat the procedure using time bases of 0.2 ms, 1 μs, and 0.01 μs and correspondingly faster data rates.

Return INTERNAL CLOCK to 0.01 μs and ARM to AUTO.

7.8 Record Mode

Set RECORD to PRETRIGGER and DELAY/CURSOR to DELAY. Increment the pretrigger delay counter to 999. As the count is increased, the trigger marker will appear at the left edge of the display and move across to the right. The trigger marker should move smoothly across the display. When a count of 999 is reached, the counter will roll over and start again at 000. Decrement the counter through 000. It should roll back to 999 and continue down to 000, where it should stop.

Set RECORD to CLOCK DELAY. The delay counters should show 0000 on the front panel display. Increment the delay counter to 9999. The data will move smoothly across the display. When a count of 9999 is reached, the display will stop moving and the counter should not roll over. Decrement the counter to 0000.

Set RECORD to EVENTS DELAY and INTERNAL CLOCK to 0.02 μs. Increment the delay counter toward 9999. As the count is increased, the display should begin to flicker

as more and more events are counted. Decrement the counter to 0000.

Set pulse generator to manual trigger. Set 9100-D delay counter to 0010. Select ARM to SINGLE. Manually arm unit. Display should blank. Manually trigger the pulse generator ten times. The display should still be blank. Manually trigger the pulse generator one more time. The display should return.

Decrement counter to 0000. Set ARM to AUTO and INTERNAL CLOCK to 0.01 μs. Return RECORD to PRETRIGGER.

7.9 Delay/Cursor

Momentarily press the INCREMENT switch once. The delay display should increase by only one. Verify that the delay can be single stepped by momentarily pushing the INCREMENT or DECREMENT switch.

Verify that the delay display counts all digits in the units, tens, hundreds, and thousands position. When the INCREMENT/DECREMENT switch is held in either position, the delay count should have three separate speeds. The speed will increase, in steps, the longer the switch is held on.

Set DELAY/CURSOR display to CURSOR. Increment the display count and check all digits as in the preceding step.

Increment cursor to 010. Set DELAY/CURSOR display to DELTA CURSOR (△CURSOR). Set the delta cursor marker. Increment the cursor to 989 while checking all the digits in the units, tens, and hundreds position. CLEAR the delta cursor marker, then SET the delta cursor marker. When the cursor is cleared, the delay display will go to 000. The delta cursor will count from this position.

When the delta cursor marker is set, the marker should appear on the display. When it is cleared, it should disappear from the display.

7.10 Input Data Speed

7.10.1 Latch TTL

Remove inputs to all channels.

Set INPUT MODE for channels 1-4 and 5-9 to LATCH. Set both thresholds to TTL X1. Set channels 1-9 COMBINATIONAL TRIGGER to "0". Set up a 5-ns wide pulse with a base line of 0 V and a peak amplitude of 1.9 V. Set the repetition rate at 15 MHz. Input this signal through a X1 BNC cable with a 50 Ω terminator to the channel 1 BNC. Verify that the unit does not miss any pulses. Perform this procedure on channels 2-9, doing only one channel at a time.

Change thresholds to TTL X10. Input this same signal through a Biomation X10 probe and perform the same test as above.

Set threshold to TTL X1. Set up a negative 5-ns wide pulse with a base line of +3 V and an amplitude of -2.10 V (signal should go from 3 V to 0.9 V). Use the same repetition rate as before. Individually check each channel for missing pulses.

Change thresholds to TTL X10. Input this negative-going signal through a Biomation X10 probe and perform the same test as above.

To complete the Latch mode test, check both ECL thresholds for missing pulses. Sample Mode should also be tested. Refer to Table 7.1 for settings of input signal.

7.10.2 Sample Mode

Use the same signals and procedures as in the Latch Mode test, except make all pulses 14-ns wide.

Table 7.1 Latch Mode

Threshold	Signal	Signal Level	Pulse Width	Repetition Rate	Combinational Trigger
TTL X1	Positive	0 V to +1.9 V	5 ns	15 MHz	"0"
	Negative	3 V to +0.9 V	5 ns	15 MHz	"0"
TTL X10	Same signal as TTL X1, input through a Biomation X10 probe.				
ECL X1	Positive	-1.8 to -0.8	5 ns	15 MHz	"1"
	Negative	-0.8 to -1.8	5 ns	15 MHz	"1"
ECL X10	Same signals as ECL X1, input through a Biomation X10 probe.				

SECTION VIII

SCHEMATICS AND ASSEMBLY DRAWINGS

8.1 Introduction

This section contains the schematics and assembly drawings for the Model 9100-D. Parts lists are also included for user convenience.

8.2 List of Drawings

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8.3 Parts Lists

The materials in the following lists are subject to change without Gould Inc.'s prior notification. For list verification, contact the Customer Service Department at the factory: Phone (408) 988-6800 TWX 910-338-0509.

8.3.1 List of Parts Lists

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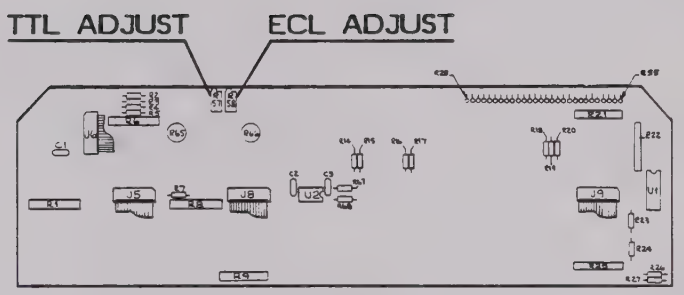
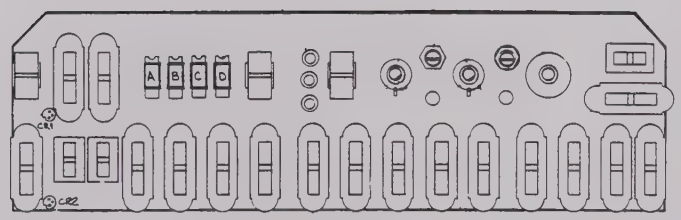
Control Board Assembly	63
Main Board Assembly	65



COMPONENT SIDE



SOLDER SIDE

Figure 8.1 Front Panel Assembly

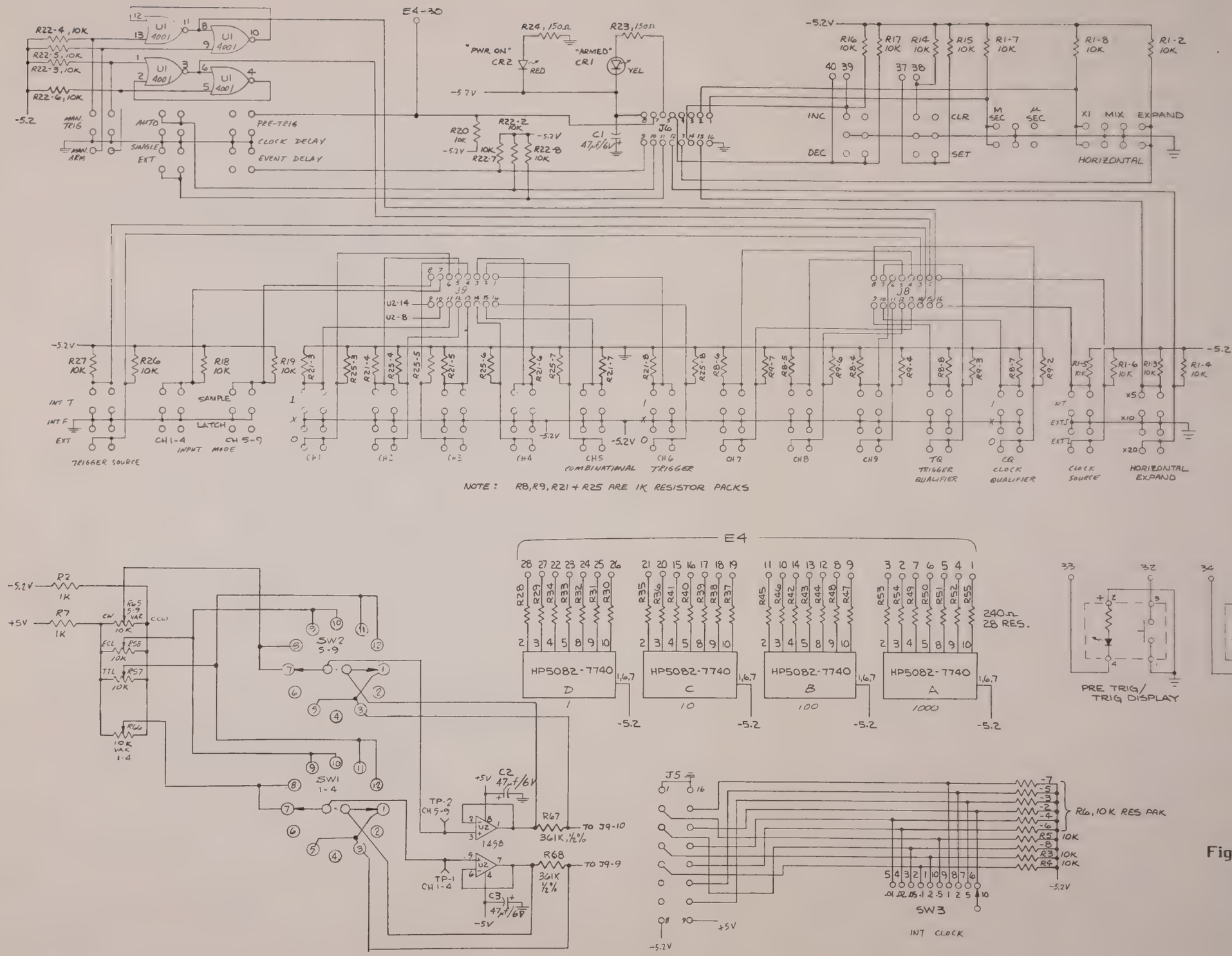


Figure 8.2 Front Panel Schematic

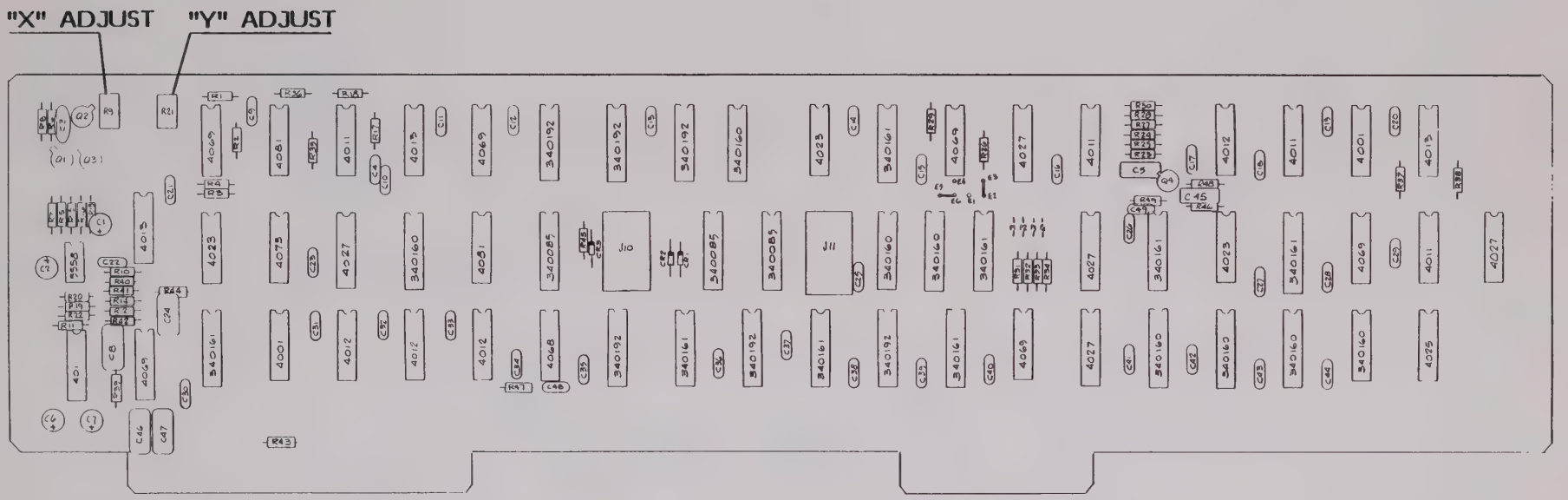


Figure 8.3 Control Board Assembly

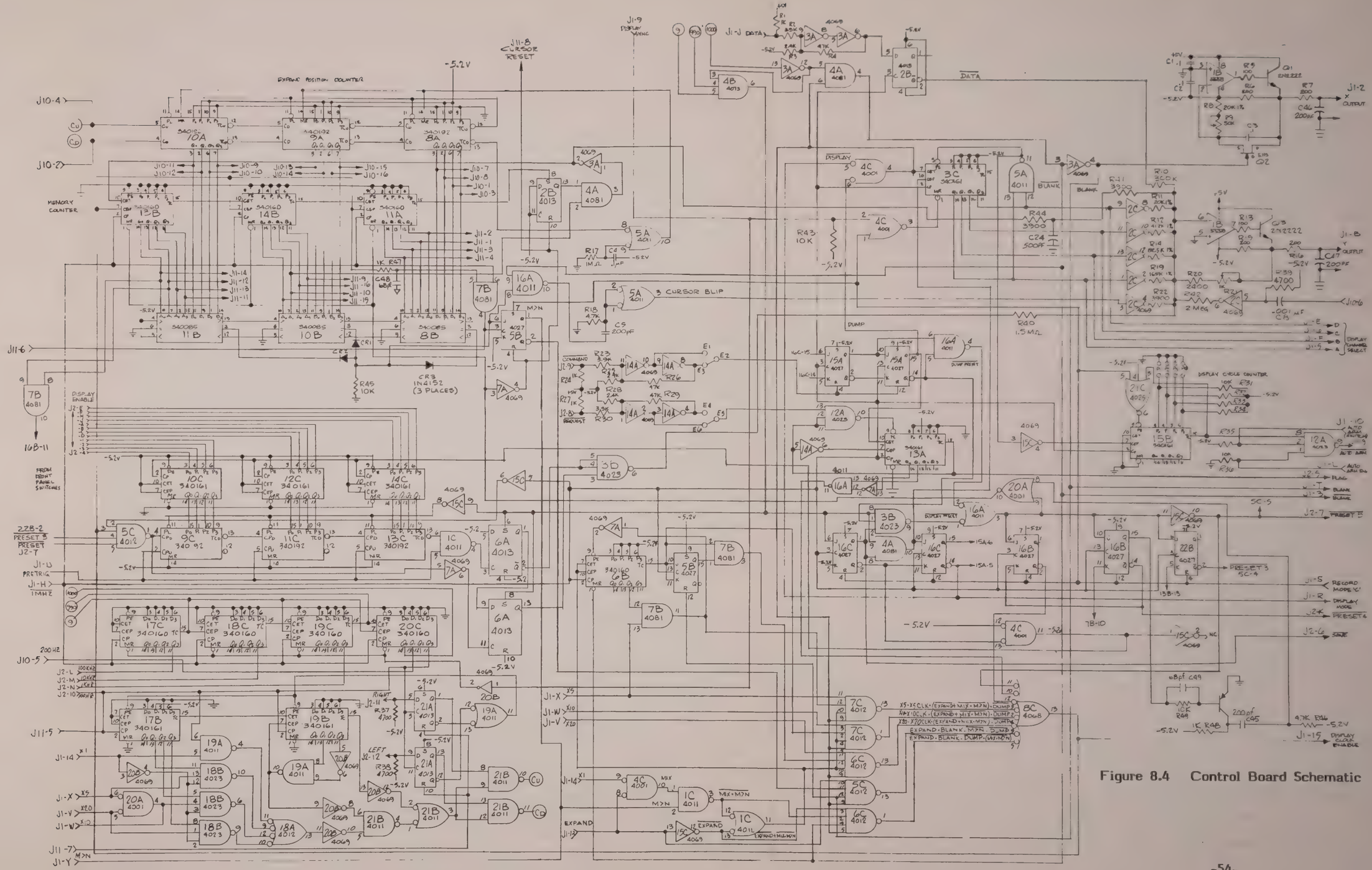


Figure 8.4 Control Board Schematic

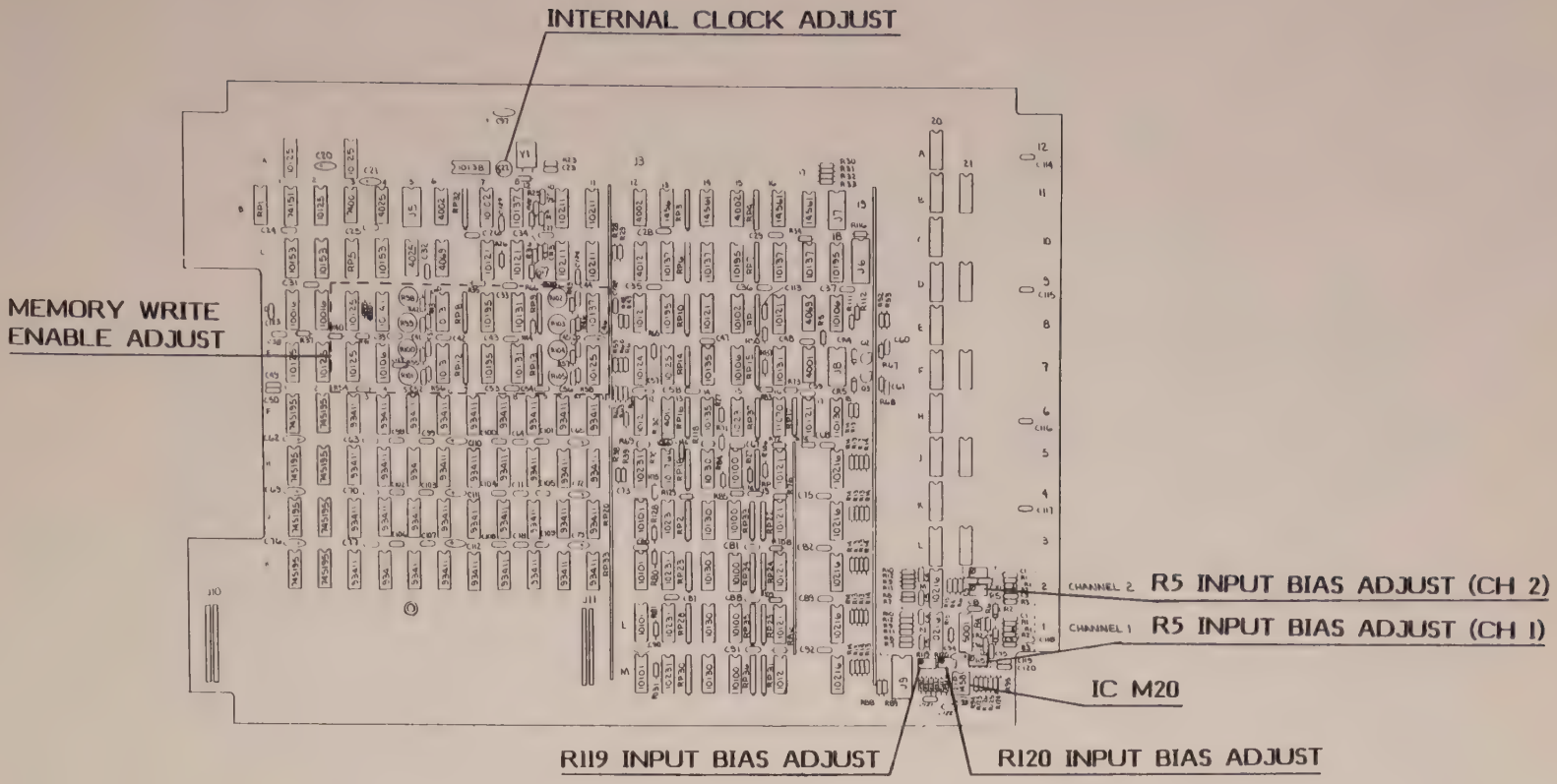


Figure 8.5 Main Board Assembly

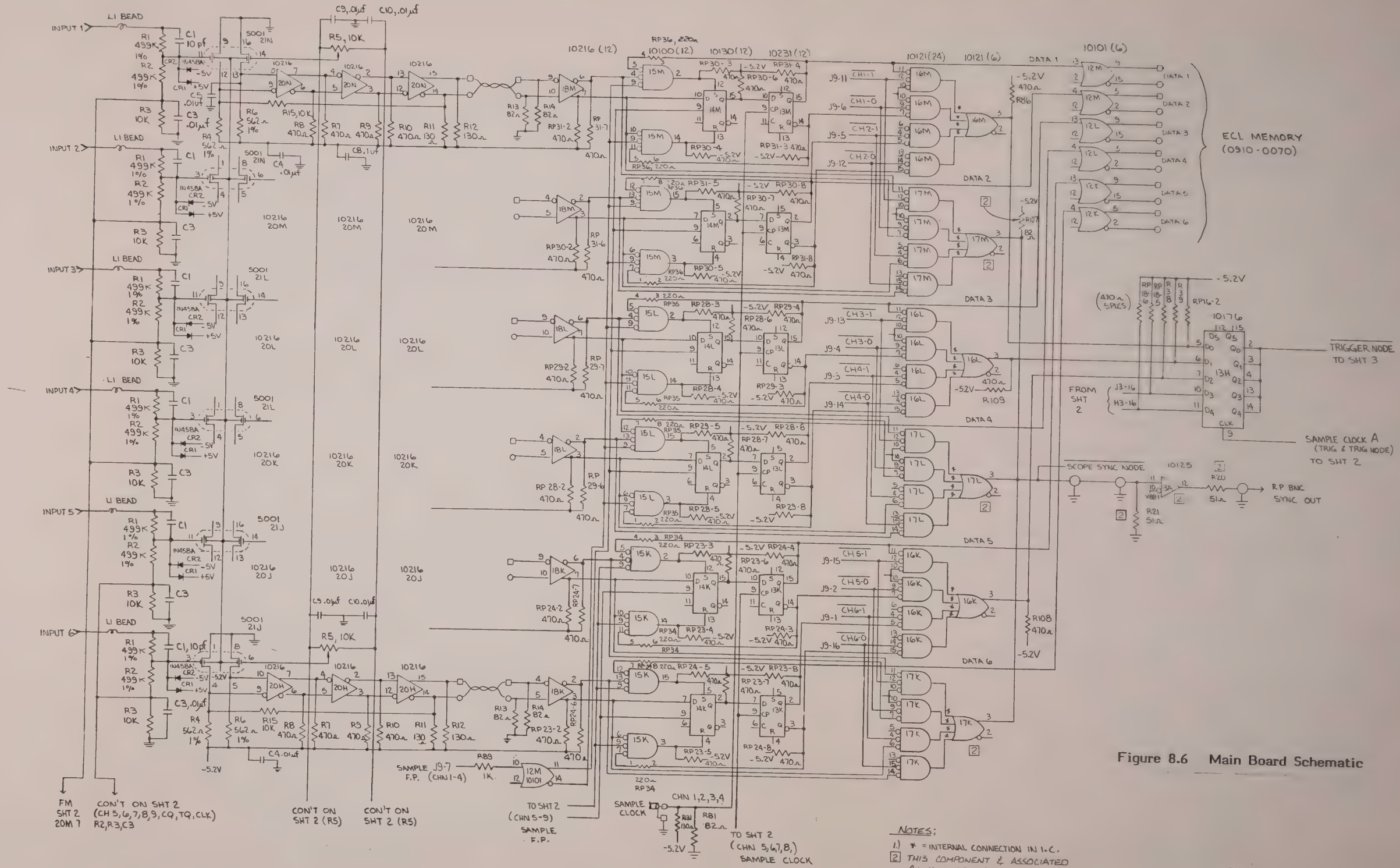


Figure 8.6 Main Board Schematic

NOTES:

1) * = INTERNAL CONNECTION IN I.C.
2) [2] THIS COMPONENT & ASSOCIATED SIGNALS ARE OPTIONS ONLY.

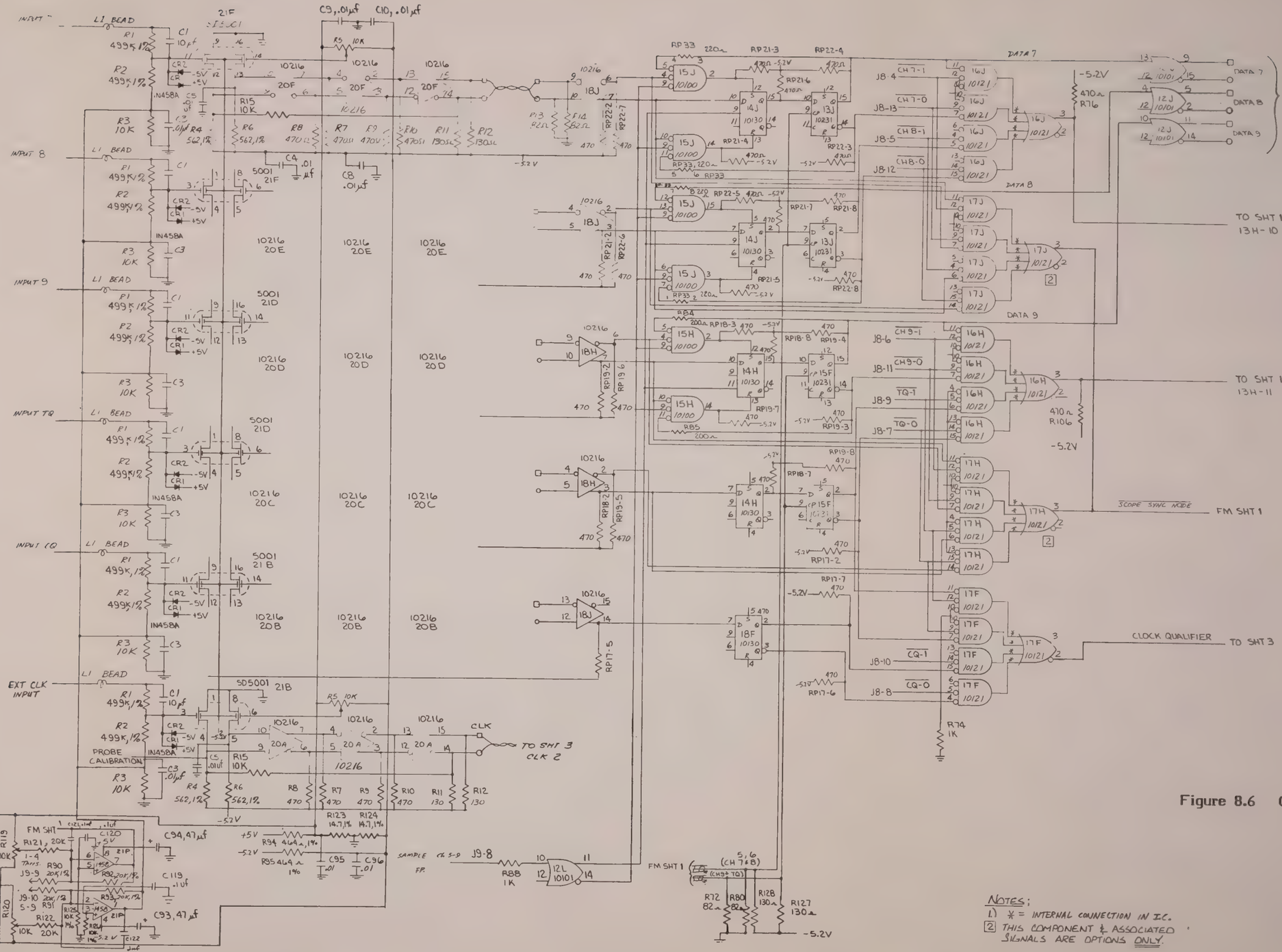


Figure 8.6 Cont. Main Board Schematic

NOTES;
1) * = INTERNAL CONNECTION IN IC.
2 THIS COMPONENT & ASSOCIATED SIGNALS ARE OPTIONS ONLY.

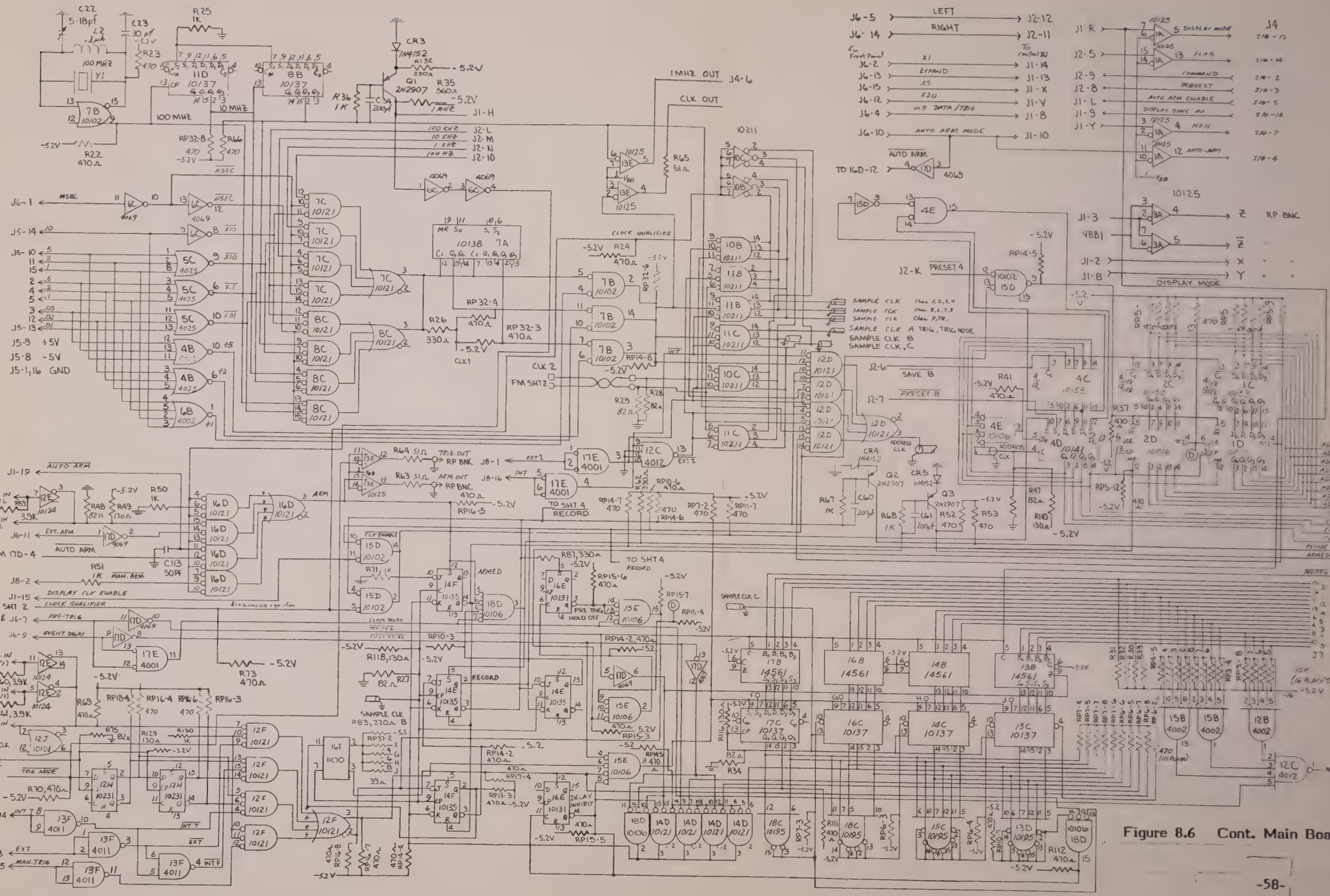


Figure 8.6 Cont. Main Board Schematic

Figure 8.6 Cont. Main Board Schematic

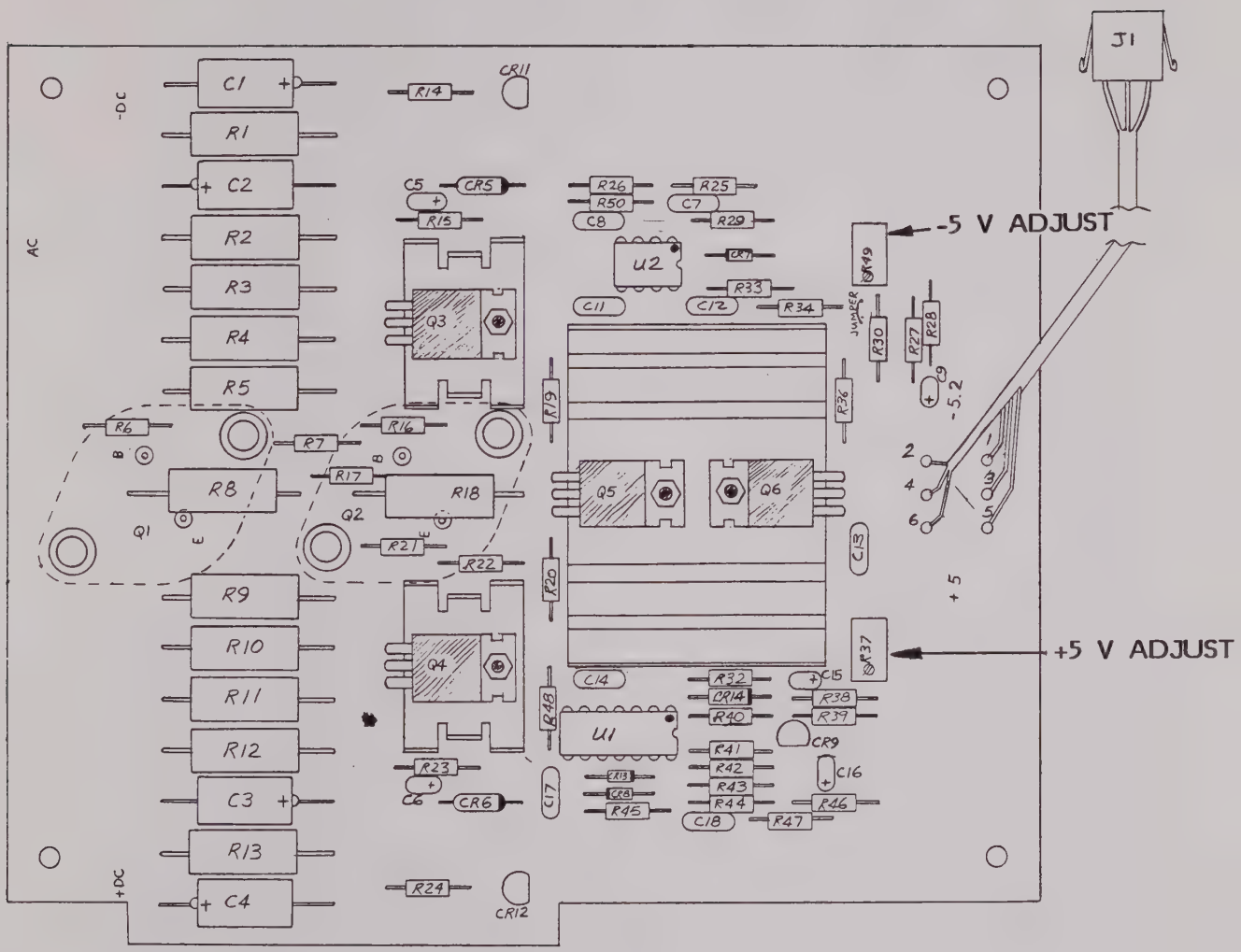


Figure 8.7 Power Supply Regulator Board Assembly

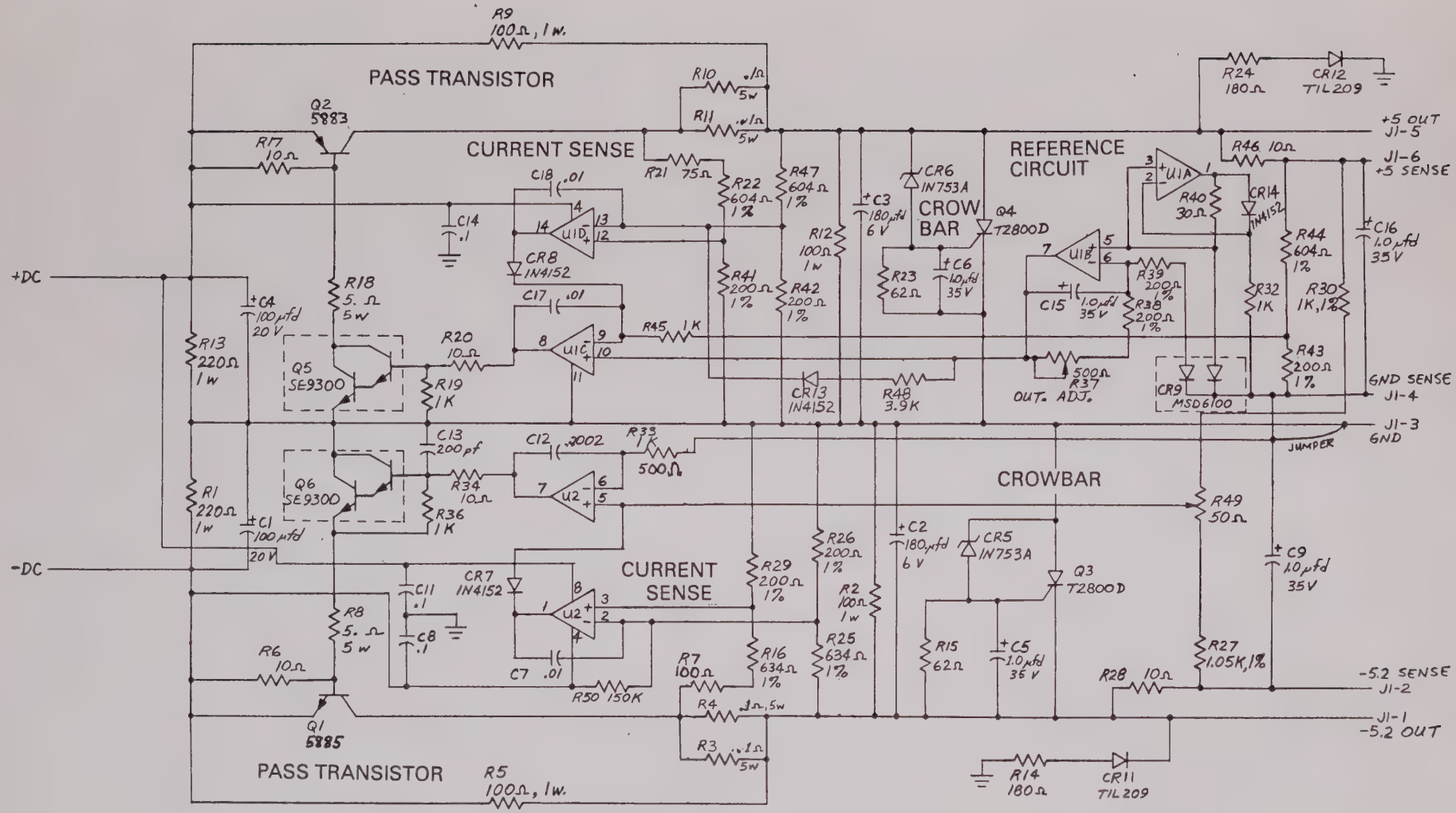


Figure 8.8 Power Supply Schematic

Front Panel PWB Assembly 0910-0025

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
1						1	0910-0027-10	FT PANEL PWB				
2						3	6600-0068	PADDLE SWITCH		C&K 7215-C-32-V30	(ON) ON (ON) WITH BKT	
3						17	6700-0008	SLIDE SWITCH		C-W A-328, 602-65, 620-42	DP 3T	
4						3	6700-0012	SLIDE SWITCH		C-W S-326, 6-02-65, 6-20-42	2P DT WITHOUT CAPS	
5						1	6A00-0039	LED RED	CR2	HP 5082-4684		
6						1	6400-0040	LED YEL	CR1	HP 5082-4584		
7						2	6100-0070	TRAN, SOCLET		AUGAT 8060-167	FOR LEDS	
8						3	0820-0105-70	FLAT CABLE	J6,8,9	CA-D-16P-02 -26-1-D6-11	16P DIP 1" LONG	
9						9	3000-1002	RESISTOR	R14,15,16,17,18,19, 20,26,27		10K 5% 1/4W	
10						2	3000-1500	RESISTOR	R23,24		150Ω 5% 1/4W	
11						4	3700-0016	RESISTOR, PACKAGED	R8,9,21,25		1K, 8 PIN	
12						3	3700-0015	RESISTOR, PACKAGED	R1,6,22		10K, 8 PIN	
13						1	1820-0001	IC	U1	4001		
14						3	6600-0074	SWITCH/INDICATOR		TECLITE SSBL-A05-A-W02		
15						4	6400-0043	DISPLAY	A,B,C,D	HP 5082-7740	7 SEGMENT LED	
16						4	6100-0113	IC SOCKET			14 PIN WIRE-WRAP	
17						2	3500-1023	POTENTIOMETER	R65,66			
18						1	6900-0008	SWITCH				
19						2	6000-0041	TEST POINT			BLACK	
20						2	7000-0136	STANDOFF			MALE/FEMALE 8-32 x 1 3/8 LG.	
21						C		KEP NUT			#8	
22						2	3300-0070	POT	R57,58	64Z103	10K, 20T	
23						28	3000-2400	RESISTOR	R28-55		240Ω, 1/4W, 5%	
24						1	7000-0379	NYLON WASHER	@ R65		.385 I.D., .625 O.D.	
25												
26												
27						2	3100-1001	RESISTOR	R2,7		1K 1/8W, 1%	
28						3	4300-0025	CAPACITOR	C1,2,3		47μF 6V	
29						2	3120-3613	RESISTOR	R67,68		361K, 1/2%	
30						1	1820-0018	IC	U2	1458P	8 PIN DIP	
31						1	9000-0002-30	FLAT CABLE	J5		16PN DIP 16" LG	
32						2	0910-0009	ROTARY SWITCH	SW1,2	12 RB-6 PC RCL ELECT.	6 POLE, 2 POSITION	
33												
34						A/R		WIRE	TO R65 R66	WHITE	24GA STRANDED	
35												
36												

Control Board Assembly 0910-0015

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
1						1	0910-0017	P.W. BOARD				
2												
3						2	1820-0001	INTEGRATED CCT.	4C, 20A		4001	
4						5	1820-0003	"	1C, 5A, 16A, 19A, 21B		4011	
5						4	1820-0004		5C, 6C, 7C, 18A		4012	
6						3	1820-0017		2B, 6A, 21A		4013	
7						3	1820-0006		3B, 12A, 18B		4023	
8												
9						5	1820-0008		5B, 15A, 16B, 16C, 22B		4027	
10						1	1820-0062		8C	FAIRCHILD	4068	
11						6	1820-0010		2C, 3A, 7A, 14A, 15C, 20B		4069	
12						1	1820-0031		4B		4073	
13						2	1820-0030		4A, 7B		4081	
14						1	1820-0007		21C		4025	
15						4	1820-0043		11A, 13B, 14B, 17C	FAIRCHILD ONLY	340160	
16						4	1820-0013		6B, 18C, 19C, 20C		340160	
17						8	1820-0014		3C, 10C, 12C, 13A, 15B, 14C, 17B, 19B		340161	
18						3	1820-0012	INTEGRATED CCT.	8B, 10B, 11B		340085	
19						6	1820-0015	INTEGRATED CCT.	8A, 9A, 10A, 9C, 11C, 13C		340192	
20												
21						1	1700-0018	INTEGRATED CCT.	1B		5558	
22												
23						3	6100-0046	16 PIN DIP SOCKET	J10, 11, 22B			
24												
25						2	3000-1000	RESISTOR	R5, 13		100Ω, 1/4W, 5%	
26						4	3000-2000	"	R6, 7, 15, 16		200Ω, " "	
27						5	3000-1001		R1, 24, 27, 47, 48		1000Ω	
28						4	3000-2401		R3, 25, 28, 20		2400Ω	
29						6	3000-3901		R2, 22, 23, 30, 41, 44		3900Ω	
30						1	3000-1504		R40		1.5MΩ	
31						5	3000-4701		R18, 37, 38, 39, 46		4700	
32						9	3000-1002		R31, 32, 33, 34, 35, 36 43, 45, 49		10K	
33						3	3000-4702		R4, 26, 29		47K	
34						1	3000-3003		R10		300K " "	
35						1	3000-1004	RESISTOR	R17		1MΩ, 1/4W, 5%	
36						1	3000-2004	RESISTOR	R42		2MEG, 1/4W 5%	

ITEM	QUANTITY PER ASSEMBLY						PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
	-60	-50	-40	-30	-20	-10						
37						2	3100-2002	RESISTOR	R8,11		20K, 1/8W, 1%	
38						1	3100-4122		R12		41.2K	
39						1	3100-8252		R14		82.5K	
40						1	3100-1653		R19		165K, 1/8W, 1%	
41						1	1490-0011	TRANSISTOR	Q4		2N4959	
42						2	4100-0024	CAPACITOR	C48,49		68 pf	
43						1	3300-0052	RESISTOR, VAR	R21		1000,	
44						1	3300-0051	RESISTOR, VAR	R9		50K.	
45						3	1000-0002	DIODE	CR1,2,3		1N4152	
46						2	1300-0001	TRANSISTOR	Q1,3		2N2222	
47						1	1500-0008	TRANSISTOR	Q2		E113	
48												
49						1	4200-0004	CAPACITOR	C3		.1MF, 100V, 10%	
50						4	4100-0008		C5,45,46,47		200PF, 500V, 10%	
51						2	4300-0025		C6,7		47MF, 6V, 10%	
52						38	4000-0025	CAPACITOR	C1,2,4,9-23,25-44		.1MF, 50V	
53						1	4000-0026	CAPACITOR	C8		.001MF, 1KV	
54						1	4100-0009	CAPACITOR	C24		500PF, 500V, 10%	

Main Board 0910-0010

ITEM	QUANTITY PER ASSEMBLY						PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
	-60	-50	-40	-30	-20	-10						
1						1	0910-0012	MAIN PCB				
2						1	0910-0070	PCB ASSY			ECL MEMORY	L/M
3						1	1820-0001	I.C	17E		4001	
4						3	1820-0002	I.C.	6B, 12B, 15B		4002	
5						1	1820-0003	I.C	13F		4011	
6						1	1820-0004	I.C	12C		4012	
7						2	1820-0007	I.C	4B, 5C		4025	
8						2	1820-0010	I.C.	6C, 17D		4069	
9						1	1800-0001	I.C.	3B		7400	
10						1	1800-0082	I.C.	1B		74151	
11						8	1800-0128	I.C.	1K, 2K, 1J, 2J, 1H, 2H, 1F, 2F,		745195	
12						36	1800-0127	I.C.	3K-11K, 3J-11J, 3H-11H, 3F-11F		87S117, 93411A	
13						5	1850-0024	I.C.	15H, 15J, 15K, 15L, 15M		10100	
14						4	1850-0037	I.C.	12J, 12M, 12L, 12K		10101	
15						2	1850-0002	I.C	15D, 7B		10102	
16						3	1850-0025	I.C.	4E, 15E, 18D		10106	
17						1	1850-0021	I.C.	12E		10124	
18						9	1850-0014	I.C.	1A, 3A, 2B, 3D, 1E, 2E, 3E, 11E, 13E,		10125	
19						11	1850-0030	I.C.	7C, 8C, 12D, 14D, 12F, 16M-16M, 17F		10121	
20						6	1850-0051	I.C.	14H-14M, 18F		10130	
21						5	1850-0006	I.C.	6E, 8E, 16E, 6D, 8D		10131	
22						2	1850-0031	I.C.	8B, 11D		10137	
23						1	1850-0041	I.C	7A		10138	
24						2	1850-0028	I.C	14E, 14F		10135	
25						1	1850-0053	I.C.	4D		10141	
26						3	1850-0054	I.C.	1C, 2C, 4C		10153	
27						4	1850-0044	I.C.	11B, 11C, 10C, 10B		10211	
28						17	1850-0043	I.C.	20A-20N 18H-18M		10216	
29						6	1850-0019	I.C.	12H, 13J-13M 15F		10231	
30						5	1850-0048	I.C.	7D, 7E, 13D, 15C, 18C		10195	
31						2	1850-0055	I.C.	1D, 2D		10016	
32						1	1700-0018	I.C.	21P		MC1458	
33						1	1850-0047	I.C.	16F		11C70	
34						4	1800-0011	I.C.	13B, 14B, 16B, 17B		14561	
35						6	1500-0012	F.E.T.	21B, 21D, 21F, 21J, 21L 21N		SD 5001	
36						1	1850-0062	I.C.	13H	CERAMIC CASE "L"	10176L	

ITEM	QUANTITY PER ASSEMBLY						PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
	-60	-50	-40	-30	-20	-10						
37						12	4100-0005	CAPACITOR	(C1X12x)		10 pf, 5%, 500V	
38						4	4100-0006	"	C41,45,52, 56		20pf, 5%, 500V	
39						3	4100-0008	"	C34, C60, C61		200pf, 5%, 500V	
40						5	4100-0019	"	C40, 44, 51, 55 C113		50pf, 5%, 500V	
41												
42						1	4600-0001	"	C22	JFD DV11PS	5-18pf	
43						16	4300-0025	"	C20, 21, 46, 51, 62, 65, 68 72, 76, 79, 94, 97, 110-112		47μf, 6V, 10%	
44						112	4000-0038	"	C24-29 (C32 C101 66) C31-33, 35-39, 42, 43, 47-50 53, 54, 58, 59, 63, 64, 66-68		.01μf	
X									70-74, 77-75, 77, 78, 80-82, 87-92, (C3, C4, C5 (12x) 95, 96, 98-103, C14-C18			
46						1	4100-0029		C23		30pf, 5%, 500V	
47						4	1850-0061		13C, 14C, 16C, 17C	FAIRCHILD ONLY	10137	
48						16	4000-0025		(C8 (6X) C119, C120 C121-128		.1uf	
49						8	3000-3006	RESISTOR	R42, 43, 45, 46, 55-58		30Ω, 1/4W, 5%	
50						3	3000-5106	"	R63-65		51Ω, 1/4W, 5%	
51						32	3000-8206	"	(R13, R14Y11x) 29, 34, 47, 48, 28, 27, 80, 81	72, 75,	82Ω, 1/4W, 5%	
52						32	3000-1300	"	(R11, R12X(12x) 110, 49 127-129, 131, 116, 118		130Ω, 1/4W, 5%	
53						1	3000-1000	"	R54		100Ω, 1/4W, 5%	
54						1	4000-0011	CAPACITOR	C129		2.2uf	
55						68	3000-4700	RESISTOR	22, 23, 66, 69 37-39, 41, 52, 53 (R7, 8, 9, 10)(12x) 70, 73	108, 109 76, 86, 06, 112, 24	470Ω, 1/4W, 5%	
56						4	3000-3300	"	R26, 62, 87, R132		330Ω, 1/4W, 5%	
57						12	3000-1001	"	R25, 36, 44, 50, 51, 61, 68, 71, 74, 88, 89, 130		1K, 1/4W, 5%	
58						3	3000-2200	"	R83, 84, 85		220Ω, 1/4W, 5%	
59						3	3000-3901	"	R59, 60, 61		3.9K, 1/4W, 5%	
60						28	3000-1002	"	R3, R15 (12X) R30-33,		10K, 1/4W, 5%	
61						6	3100-2002	"	R90-93, 121, 122		20K, 1/8W, 1%	
62						24	3100-5620	"	(R4, R6)(12x)		562Ω, 1/8W, 1%	
63						24	3100-4993	"	(R1, R2,)(12x)		499K, 1/8W, 1%	
64						14	3300-0046	" POT	(R5)(12x), 119, 120	SPECTROL 64Y103	10K, 20 TURNS	
65						8	3300-0063	" POT	R98-105	STERLING ELEC E086BD2K2	2.2K, ±20%	
66						2	3100-4640	"	R94, 95		464Ω, 1/8W, 1%	
67						2	3100-1476	"	123, 124		14.7Ω, 1/8W, 1%	
68						1	3000-7500	"	R40		750, 1/4W, 5%	
69						2	3100-1002	"	R125, 126		10K, 1/8W, 1%	
70						1	3000-5600	RESISTOR	R35		560Ω, 1/4W, 5%	
71												
72												

Cont. Main Board 0910-0010

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
73						1	3700-0027	RESISTOR PACK	RP1	BECKMAN 898-1-R330	330Ω, 16 PIN	
74						1	3700-0004	"	RP5	BECKMAN 898-1-R470	470Ω, 16 PIN	
75						4	3700-0044	"	RP33-36		220Ω, 8 PIN	
76						1	3700-0043	"	RP37		39Ω, 8 PIN	
77						2	3700-0015	"	RP3, RP4	BECKMAN 784-1-R10K	10K, 8 PIN	
78						23	3700-0021	"	RP6-19, RP21-24, RP28-32	BECKMAN 784-1-R470	470Ω, 8 PIN	
79												
80						24	1000-0017	DIODE	(CR1 & CR2 (12x)		IN458A	
81						3	1000-0002	DIODE	CR3, 4, 5	T.I.	IN4152	
82						3	1400-0001	TRANSISTOR	Q1, 2, 3	T.I.	2N2907	
83						1	2100-0014	INDUCTOR	L2	DELEVAN	.1μh	
84						1	5100-0004	CRYSTAL	Y1	MONITOR PRODUCTS	100 MHZ	
85						12	2100-0001	FERRITE BEAD	L1 (12x)	FERROXCUBE K500100/3B		
86						5	6100-0020	FASTENER	J5, 6, 7, 8, 9	CA-16-200	FOR 16 PIN SOCKET	
87						1	7000-0167	STANDOFF		HHS 8323	1/4 O.D., ALUM 1/2 LG	
88												
89						4	6000-0224	CONNECTOR	J10, J11	MOLEX 22-04-2151	15 PINS	
100												
101						5	6100-0019	SOCKET	J5, 6, 7, 8, 9	CA-165-1050	16 PIN	
102						1	6100-0021	SOCKET	J3	AMP 1-380999-0	6 PIN	
103						1	6000-0007	CONNECTOR	J4	AMP #57-40240	24 PIN	
104						2	0850-0150-19	BUSS BARS			20 PINS	
105						1	0850-0150-80	BUSS BARS			5 PINS	
106						1	6000-0019	CONNECTOR	J1	CINCH 50-44B-10	22 PIN DUAL	
107						1	6000-0020	CONNECTOR	J2	CINCH 50-24B-10	12 PIN DUAL	
108						1	0910-0035	FRONT BRACKET				
109						1	0910-0036	REAR BRACKET				
110						1	6000-0176	HEADER		BERG 65611-x24	12 PIN DUAL	
111						22	6000-0003	BNC		KINGS	KC-79-46	
112						1	6000-0041	TEST POINT		POMONA 3542 (BLK		
113						1	6600-0070	SWITCH	S1	ALCO STV 250 LO	EURO STD PWR SW	
114						44	———	BNC WASHER			BNC FLAT WASHER .500 O.D x .062 THK	
115						4	6200-0041	FAST TAB		PANDUIT		
116												
117												
118												

ITEM	QUANTITY PER ASSEMBLY						PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
	-60	-50	-40	-30	-20	-10						
119						1	6000-0024	CONN 4 PINS				
120						4	6100-0005	CONN PINS		AMP 61174-1	MALE	
121						1	7000-0305	NUT, HEX	FOR SWITCH	C&H Hammer #1196	BRASS, N.P., 15/32-32 5/64 THK	
122						1	6100-0118	SOCKET	21P		8 PIN SOCKET	
123						51	6100-0046	SOCKET	3E-11E, 3H-11H, 3J-11J, 3K-11K, 21B, 2D 21E, 2J 21L, 21N, 4D, 4E	AUGAT 7B, 13C-18C	16 PIN SOCKET	
124						A/R		WIRE			24 AWG, RED	
125						A/R		WIRE			24 AWG, BLK	
126						A/R		WIRE			24 AWG, GRN	
127						A/R		WIRE			24 AWG, GRY	
128						A/R		WIRE			24 AWG, WHT	
129						1	7100-0063	CABLE		ADVANCED 10CT26H7	10 T.P., RIBBON 27 IN. LG	
130						A/R		STA-STRAPS			FOR COAX CABLES	
131						A/R	8200-0002	ADHESIVE		THERMO #122		
132						2	7000-0126	HEATSINK			(FOR 13H)	
133						A/R		SLEEVING	AS REQ'D		PLASTIC	
134												
135						12		TWISTED PAIR WIRE	6 1/2 IN. LG		24 AWG, BLK & WHT	
136												
137						5	9000-0025-08	COAX CABLE	C1, C2, C3, C4, AC		8 IN.	
138						4	9000-0025-06	COAX CABLE	X, Y, Z, $\bar{Z}$		6 IN.	
139						6	9000-0025-12	COAX CABLE	1, 5, 9, A, B, C		12 IN.	
140						6	9000-0025-15	COAX CABLE	AO, AI, TO, TI1, TI2, CO		15 IN.	
141												
142												
143												
144												
145												
146												

MP MASTER
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